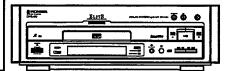


# Service Manual



ORDER NO. RRV1709

# DVL-700

#### THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Туре	Мо	del	Power requirement	Remarks
Type	DVL-90	DVL-700	Fower requirement	nemarks
KU/CA	0	0	AC120V	

• For the DVD section, refer to the service guide RRV1710 for DV-500. (The completion is scheduled for about Feb. 1997.)

#### CONTENTS

1. SAFETY INFORMATION	2
2. EXPLODED VIEWS AND PARTS LIST	3
3. SCHEMATIC DIAGRAM	18
4. PCB CONNECTION DIAGRAM	47
5. PCB PARTS LIST	66
6. ADJUSTMENT	74

7. GENERAL INFORMATION	91
7.1 PARTS	91
7.1.1 IC	91
7.1.2 DISPLAY	128
7.2 DISASSEMBLY/ASSEMBLY	129
7.3 HOW TO BEND THE FLEXIBLE CABLE	131
7.4 BLOCK DIAGRAM	132

8. PANEL FACILITIES AND SPECIFICATIONS.. 134

#### 1. SAFETY INFORMATION

This service manual is intended for qualified service technicians; It is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safety repair complex products such as those covered by this manual.

Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safety, you should not risk trying to do so and refer the repair to a qualified service technician.

#### WARNING

Lead in solder used in this product is listed by the California Health and Welfare agency as a known reproductive toxicant which may cause birth defects or other reproductive harm (California Health & Safety Code, Section 25249.5).

When serving or handling circuit boards and other components which contain lead in solder, avoid unprotected skin contact with the solder. Also, when soldering do not inhale any smoke or fumes produced.

#### NOTICE

(FOR CANADIAN MODEL ONLY)

Fuse symbols - (fast operating fuse) and/or - (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

#### REMARQUE

(POUR MODÈLE CANADIEN SEULEMENT)

Les symboles de fusible - (fusible de type rapide) et/ou - (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

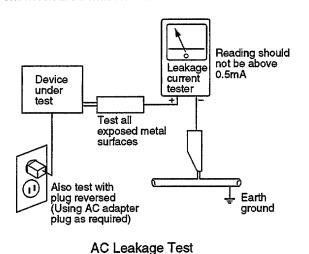
#### -(FOR USA MODEL ONLY) -

#### 1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

#### LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

#### 2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are indentified by marking with a  $\triangle$  on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

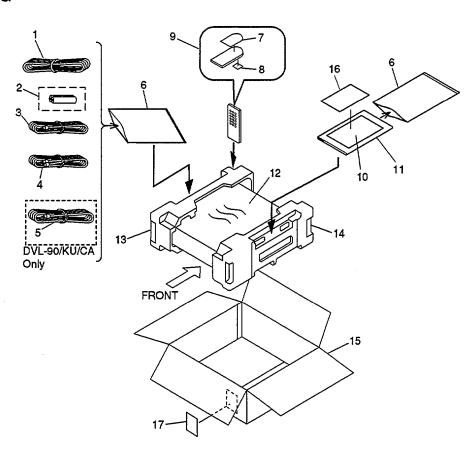
<sup>&</sup>quot;CAUTION-Laser radiation when open and interlock defeated. DO NOT STARE INTO BEAM."

## 2. EXPLODED VIEWS AND PARTS LIST

NOTES: • Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

- The  $\Lambda$  mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.

#### 2.1 PACKING



#### (1) PARTS LIST

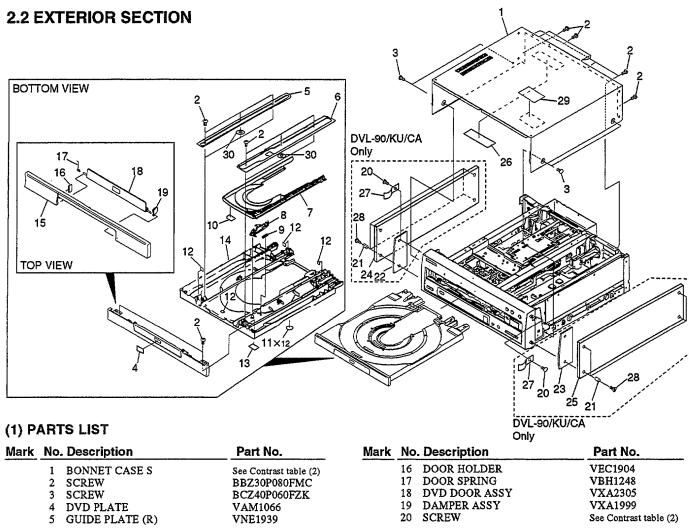
Mark	No.	. Description	Part No.	Mark	No.	Description	Part No.
MSP	3 4	AC POWER CORD DRY CELL BATTERY(R03,AAA) VIDEO CORD AUDIO CORD S VIDEO CABLE	ADG1126 VEM-022 See Contrast table (2) See Contrast table (2) See Contrast table (2)	NSP		WARRANTY CARD OPERATING INSTRUCTIONS MIRROR MAT PAD L PAD R	See Contrast table (2) See Contrast table (2) VHL1018 VHA1179 VHA1180
	6 7 8	POLYETHYLENE BAG UPPER COVER BATTERY COVER PERMOTE CONTROL LINIT	Z21-038 VNK3940 VNK3864 VXX2399	NSP	15 16 17	PACKING CASE CAUTION LABEL	See Contrast table (2) VRM1063 VRW1629

#### (2) CONTRAST TABLE

(CU-DV001)

DVL-90/KU/CA and DVL-700/KU/CA have the same construction except for the following :

		Complet & Description	Par	Remarks	
Mark	No.	Symbol & Description	DVL-90/KU/CA	DVL-700/KU/CA	Remarks
NSP	4 5 10	VIDEO CORD AUDIO CORD S VIDEO CABLE WARRANTY CARD OPERATING INSTRUCTIONS (ENGLISH)	VDE1024 VDE1023 VDE1013 ARY1026 VRB1177	VDE1036 VDE1033 Not used ARY1044 VRB1178	
	15	PACKING CASE	VHG1642	VHG1643	



IVIGIA	NU	. Description	Fait No.	IVIGIA	140	. Description	Part No.
	1 2	BONNET CASE S SCREW	See Contrast table (2) BBZ30P080FMC		16 17	DOOR HOLDER DOOR SPRING	VEC1904 VBH1248
	3	SCREW	BCZ40P060FZK		18	DVD DOOR ASSY	VXA2305
	4	DVD PLATE	VAM1066		19	DAMPER ASSY	VXA1999
	5	GUIDE PLATE (R)	VNE1939		20	SCREW	See Contrast table (2)
	6	GUIDE PLATE (L)	VNE1938		21	WOOD COLLER	See Contrast table (2)
	7	CD TRAY	See Contrast table (2)		22	DECORATION PLATE L	See Contrast table (2)
	8	LOCK PLATE	VNL1703		23	DECORATION PLATE R	See Contrast table (2)
	9	LOCK PLATE SPRING	VBH1188		24	SIDE WOOD L	See Contrast table (2)
	10	TRAY LABEL	VRW1628		25	SIDE WOOD R	See Contrast table (2)
	11	CUSHION	VEC1682		26	65 LABEL	ORW1069
	12	DAMP CUSHION	VEC1683		27	EARTH PLATE	See Contrast table (2)
NSP	13	CARRY LABEL	VRW1289		28	SCREW	See Contrast table (2)
	14	LD TRAY ASSY	See Contrast table (2)		29	LABEL	VRW1648
	15	TRAY PANEL	See Contrast table (2)		30	WASHER	VEC1254

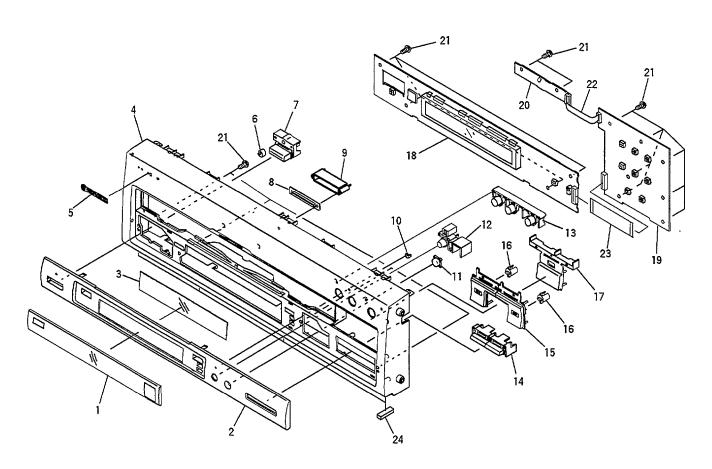
#### (2) CONTRAST TABLE

DVL-90/KU/CA and DVL-700/KU/CA have the same construction except for the following :

Mark	No.	Symbol & Description	Par	Remarks	
mair	140.	Symbol & Description	DVL-90/KU/CA	DVL-700/KU/CA	Remarks
	1	BONNET CASE S	VXX2484	VXX2485	
	. 7	CD TRAY	VNK3923	VNK3922	
	14	LD TRAY ASSY	VXA2318	VXA2173	
	15	TRAY PANEL	VNK3803	VNK3990	
	20	SCREW	BBZ30P080FMC	Not used	
	21	WOOD COLLER	PNW1238	Not used	
	22	DECORATION PLATE L	VAH1270	Not used	
	23	DECORATION PLATE R	VAH1269	Not used	
	24	SIDE WOOD L	VAP1028	Not used	
	25	SIDE WOOD R	VAP1029	Not used	
	27	EARTH PLATE	VNE1518	Not used	
	28	SCREW	IBZ40P200FZK	Not used	}

4

#### 2.3 FRONT PANEL SECTION



#### (1) PARTS LIST

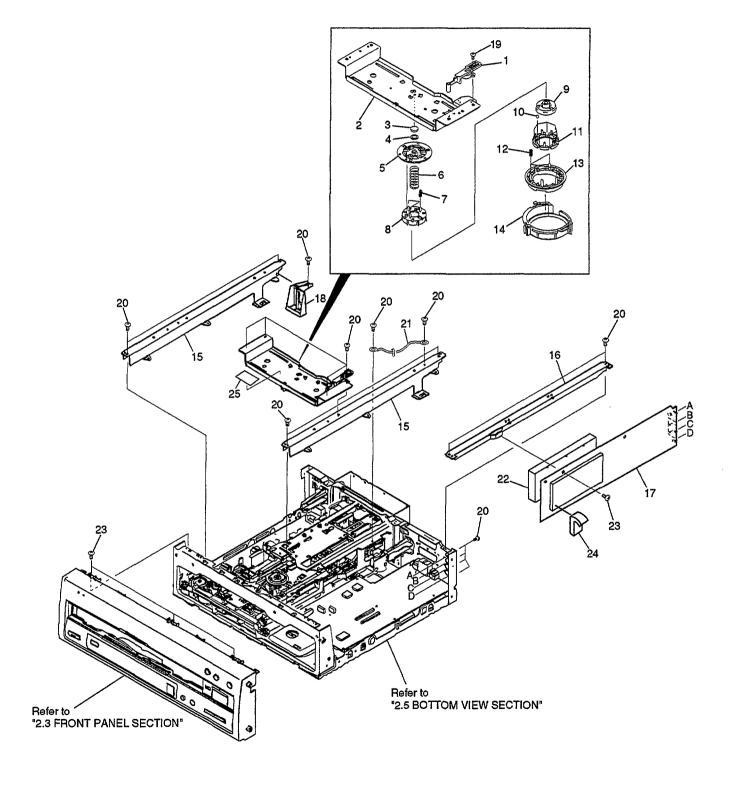
Mark	No.	. Description	Part No.	<u>Mark</u>	No	. Description	Part No.
	1	FL LENS	VNK3599		11	IR WINDOW	VNK2246
	2	SUB PANEL	See Contrast table (2)		12	DISPLAY BUTTON	VNK3694
	3	FL FILTER	VEC1890		13	OPEN BUTTON	VNK3690
	4	FRONT PANEL	See Contrast table (2)		14	SKIP BUTTON	See Contrast table (2)
	5	NAME PLATE	See Contrast table (2)		15	SIDE BUTTON	See Contrast table (2)
	6	LED LENS	PNW2019		16	SIDE LENS	VNK3602
	7	POWER BUTTON	VNK3689		17	PLAY BUTTON	See Contrast table (2)
	8	ILLUMINATION LENS	VNK3652		18	FLPB ASSY	See Contrast table (2)
	9	LED HOLDER	VNK4001		19	KEYB ASSY	VWG1736
	10	LED LENS 1	RNK2066		20	LEDB ASSY	VWG1832
					21	SCREW	BBZ30P080FMC
					22	FLEXIBLE CABLE (5P)	VDA1590
					23	FLEXIBLE CABLE (19P)	VDA1603
				NSP	24	SPACER A	VEC1933

#### (2) CONTRAST TABLE

DVL-90/KU/CA and DVL-700/KU/CA have the same construction except for the following :

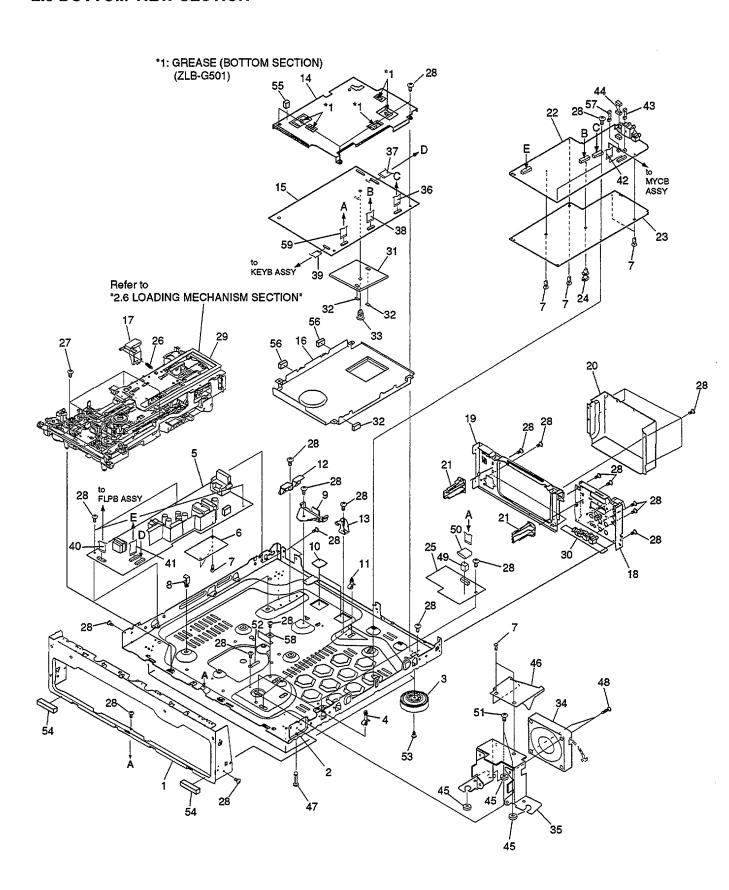
Mark	No.	Symbol & Description	Par	<b>D</b>	
Wark	140.	Symbol & Description	DVL-90/KU/CA	DVL-700/KU/CA	- Remarks
	2	SUB PANEL	VNK3685	VNK3805	
	4	FRONT PANEL	VNK4028	VNK4029	
i	5	NAME PLATE	VAM1032	PAM1704	
	14	SKIP BUTTON	VNK3807	VNK3693	
	15	SIDE BUTTON	VNK3808	VNK3925	
	17	PLAY BUTTON	VNK3806	VNK3924	
	18	FLPB ASSY	VWG1801	VWG1800	1

#### 2.4 TOP VIEW SECTION



Mark No	. Description	Part No.	<u>Mark</u>	No	. Description	Part No.
1	D LEVER ASSY	VXA2205		11	BALL GUIDE	VNL1616
2	CENTER PLATE	VNE2051		12	CLAMP SPRING	VBH1239
3	RUBBER SHEET	VEB1114		13	CLAMPER	VNL1604
4	THRUST HOLDER	VNL1663		14	CLAMPER HOLDER	VNL1708
5	CLAMPER HEAD	VNL1603	NSP	15	CENTER ANGLE	VNE2048
6	LD SPRING	VBH1240	NSP	16	PCB HOLDER	VNE2049
7	COVER SPRING	VBH1234		17	MYCB ASSY	VWV1519
8	BALL COVER	VNL1602		18	SHIPPING CAM	VNL1729
9	LD HAB	VNT1047		19	SCREW	PBZ20P060FMC
10	STEEL BALL	VNX1013		20	SCREW	BBZ30P080FMC
			NSP	21	WIRE	DE007VF0
			•	22	SHIELD CASE B	VNF1099
				23	SCREW	IBZ30P080FMC
				24	CUSHION	VEC1925
				25	FUSE CAUTION LABEL	VRW1642

#### 2.5 BOTTOM VIEW SECTION



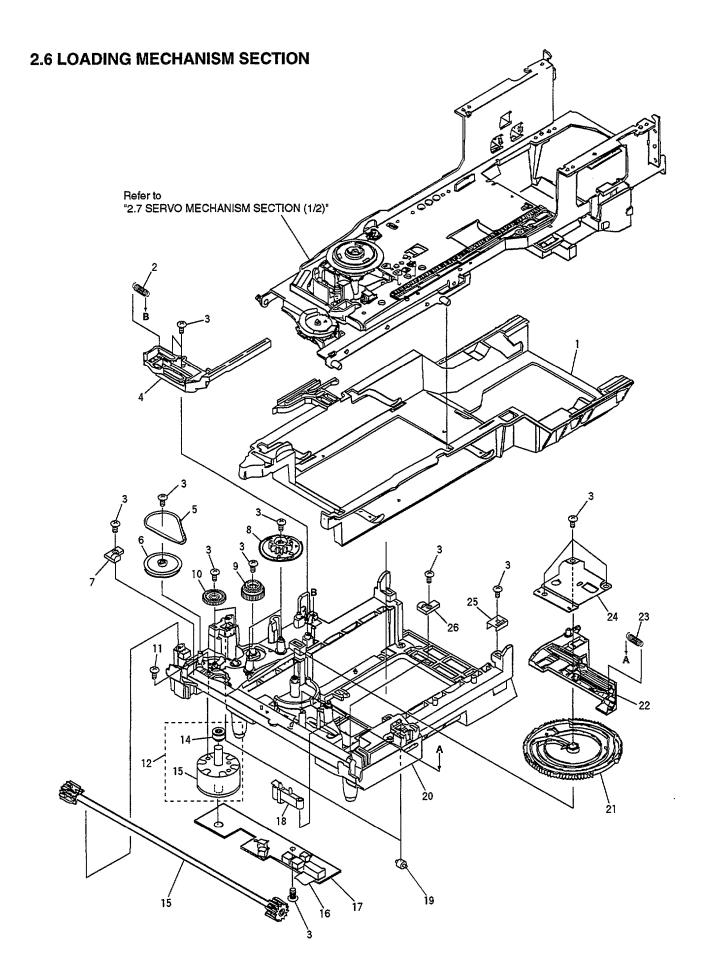
#### (1) PARTS LIST

Mark	No.	Description	Part No.	Mark	No	. Description	Part No.
NSP	1	PANEL HOLDER	VNA1686		31	FTSB ASSY	VWS1291
NSP	2	CHASSIS	See Contrast table (2)	NSP	32	SPACER A	VEC1933
	3	INSULATOR	See Contrast table (2)		33	PCB HOLDER	AEC1534
NSP	4	SPACER 40	PNW2488		34	DC FAN MOTOR	VXM1070
$\Phi$	5	POWER SUPPLY ASSY	VWR1273		35	FAN HOLDER	VNE2108
	6	SHEET P	VEC1874			FLEXIBLE CABLE (26P)	VDA1587
	7	RIVET	RBM-003			FLEXIBLE CABLE (24P)	VDA1588
	8	PCB HINGE	VEC1174			FLEXIBLE CABLE (30P)	VDA1586
NSP	9	STOPPER	VNE2088			FLEXIBLE CABLE (13P)	VDA1589
NSP	10	RUBBER SPACER	VEB1252		40	FLEXIBLE CABLE (5P)	VDA1572
NSP	11	PCB SPACER	AEC1188			FLEXIBLE CABLE (15P)	VDA1582
NSP	12	CAM HOLDER L	VNE2089			FLEXIBLE CABLE (10P)	VDA1584
NSP	13	CAM HOLDER R	VNE2090			HOUSING ASSY (2P)	VKP2138
	14	SHIELD CASE (UPPER)	VNF1093			HOUSING ASSY (8P)	VKP2139
	15	DVD MAIN ASSY	VWS1243		45	RUBBER BUSH	VEB1164
	16	SHIELD CASE (LOWER)	VNF1094	NSP		FAN COVER	VEC1921
	17	SHIPPING LEVER	VNL1728	NSP		LOCKING CARD SPACER	VEC1596
	18	REAR PANEL L	See Contrast table (2)		48		IBZ30P150FMC
	19	REAR PANEL R	See Contrast table (2)	NSP	49	SPACER B	VEC1934
	20	REAR COVER	See Contrast table (2)	$\Phi$	50	FERRITE CORE	VTH1038
	21	TRAY STOPPER	VNL1707		51		VBA1029
	22	CLD MAIN ASSY	VWS1285	NSP	52	CORD HOLDER	ZCB-069Z
	23	SHEET C	VEC1875		53		See Contrast table (2)
NSP	24	PCB SPACER	AEC1372	NSP		CUSHION	VEC1923
	25	MCRB ASSY	VWV1544	NSP	55	SPACER C	VEC1935
	26	SHIPPING SPRING	VBH1275			CUSHION	VEC1924
	27	SCREW	BBZ30P100FMC			HOUSING ASSY (2P)	VKP2142
	28	SCREW	BBZ30P080FMC	NSP	58	<del>-</del>	VNE2110
NSP	29	MECHANISM ASSY	VWT1132		59	FLEXIBLE CABLE (26P)	VDA1621
	30	JCKB ASSY	VWV1532				

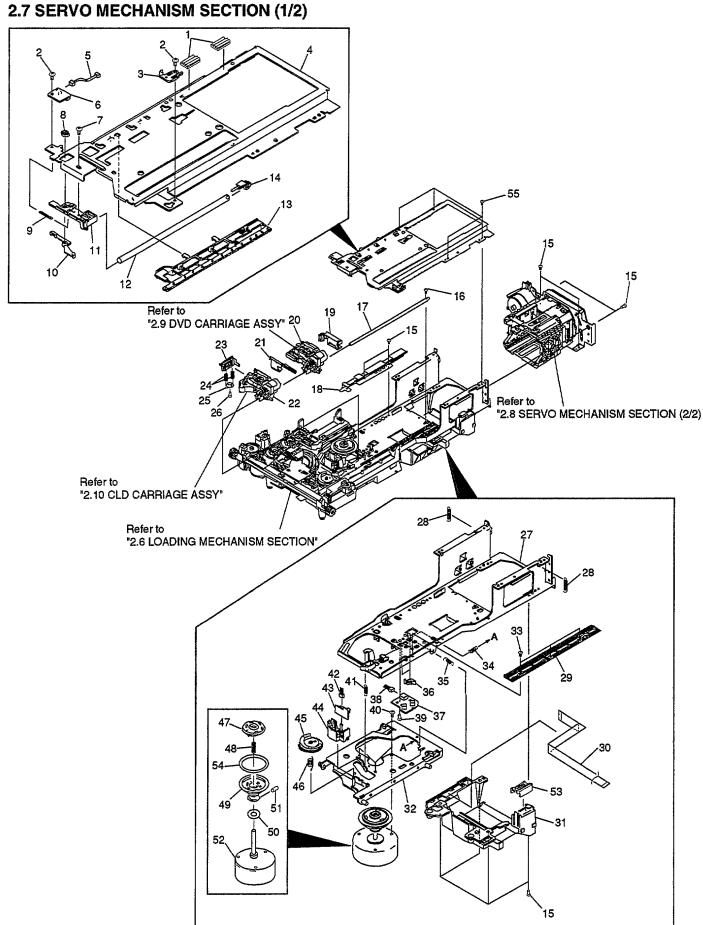
#### (2) CONTRAST TABLE

DVL-90/KU/CA and DVL-700/KU/CA have the same construction except for the following :

NoI-	A1.	Combal 9 Description	Par	Remarks	
Mark	No.	Symbol & Description	DVL-90/KU/CA	DVL-700/KU/CA	Remarks
NSP	2	CHASSIS	VNA1852	VNA1851	
	3	INSULATOR	VXA1450	PNW1912	1
	18	REAR PANEL L	VNA1718	VNA1807	
	19	REAR PANEL R	VNA1719	VNA1684	1
	20	REAR COVER	VNA1720	VNA1810	
	53	SCREW	IBZ30P150FMC	BBZ30P080FMC	

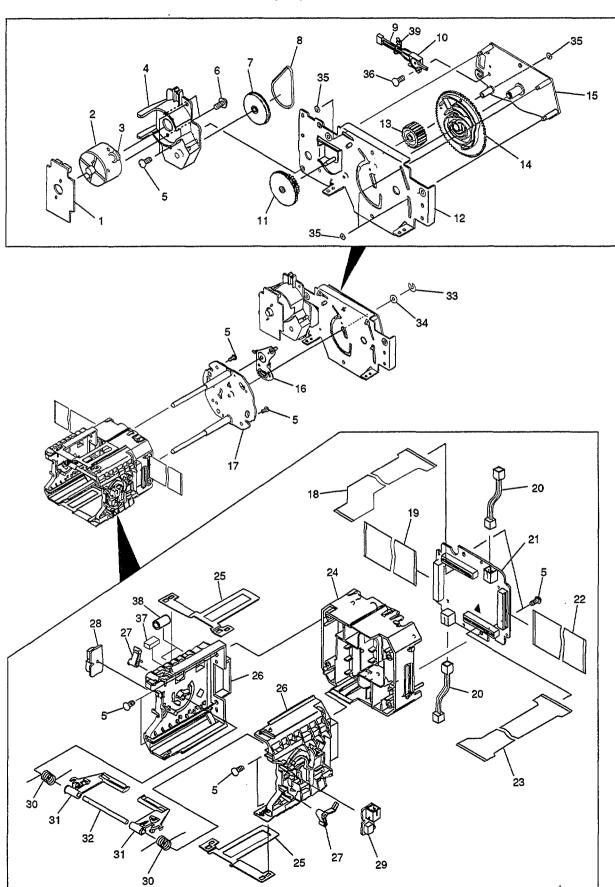


Mark	No.	Description	Part No.	Mark	k No. Description		Part No.
	1	CLAMP CAM B	VNL1765		16	FLEXIBLE CABLE (10P)	VDA1579
	2	CDP SPRING	VBH1191	NSP	17	LMSB ASSY	VWG1554
	3	SCREW	Z39-019		18	MB SWITCH LEVER	VNL1664
	4	CD PLATE	VNL1685		19	ROLLER	VNL1042
	5	RUBBER BELT	VEB1184		20	MECHANISM BASE	VNK3239
	6	GEAR PULLEY	VNL1662		21	CAM GEAR	VNL1625
	7	SLIDER(L)	VNL1665		22	CAM PLATE	VNL1631
	8	TWIN GEAR	VNL1626		23	CAS SPRING	VBH1190
	9	CENTER GEAR	VNL1660		24	SHAFT HOLDER	VNE1942
	10	DOUBLE GEAR	VNL1661		25	CAM HOLDER	VNE2032
	11	SCREW	BMZ26P040FMC		26	SLIDER(R)	VNL1666
	12	LOADING MOTOR ASSY	VXX2045				
	13	CARRIAGE MOTOR	VXM1033				
NSP	14	MOTOR PULLEY	VNL1630				
	15	SYNCHRO GEAR ASSY	VXA2105				



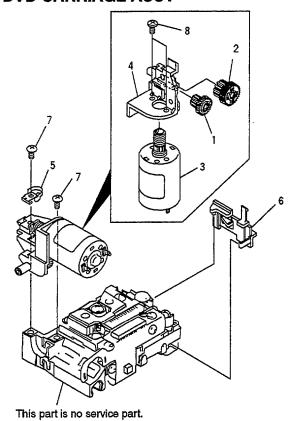
Mark	k No. Description		Part No.	Mark No. Description			Part No.	
	1	MINI CLAMP	VEC1905		26	SCREW	PMZ20P060FZK	
	2	SCREW	BBZ26P060FMC		27	TILT BASE(UNDER)	VNL1711	
	3	A HORN	VNL1689		28	TILT REAR SPRING	VBH1274	
	4	TILT BASE(UPPER)	VNE2062		29	CA RACK (LOWER)	VNL1712	
	5	HOUSING ASSY (2P)	VKP2136		30	FLEXIBLE CABLE (6P)	VDA1578	
NSP	6	BISB ASSY	VWG1796		31	FLEXIBLE CABLE COVER	VNL1727	
	7	SCREW	BPZ20P040FZK		32	MOTOR BASE	VNE1941	
	8				33	••••		
	9				34	TILT SPRING	VBH1263	
	10	SW LEVER B VNL1723			35	THRUST SPRING	VBH1245	
	11	SHAFT HOLDER	VNL1724			CA SWITCH LEVER	VNL1644	
	12	CA SHAFT(UPPER)	VLL1486	NSP		PKSB ASSY	VWG1555	
	13	CA RACK(UPPER)	VNL1722		38	HOUSING ASSY (3P)	VKP2045	
		SHAFT STAY	VNL1726		39	SCREW	IBZ26P120FMC	
	15	SCREW	BBZ30P080FMC		40	SCREW	PMA30P050FMC	
	16	SCREW	PPZ20P060FMC		41	TILT SPRING B	VBH1287	
		CA SHAFT(LOWER)	VLL1485		42	HOUSING ASSY (3P)	VKP2046	
		TAN GUIDE	VNE2061	NSP	43	FG ASSY	VWG1556	
	19	FPC HOLDER A	VNL1751		44	FG BASE	VNL1781	
	20	DVD CARRIAGE ASSY	VWT1139		45	TILT CAM	VNL1643	
	21	FPC HOLDER B	VNL1752		46	TILT CAM SPRING	VBH1243	
	22	CLD CARRIAGE ASSY	VWT1141		47	PRC HUB	VNL1684	
	23	CA GUIDE	VNL1668		48	CENTERING SPRING	VBH1269	
	24	TAN SPRING (B)	VBH1264		49	R-TURN TABLE ASSY	VXA2284	
	25	TAN LEVER(B)	VNL1669	NSP	50	OIL STOPPER	VBF1002	
						SCREW	ZMD30H030FBT	
				NSP		SPINDLE MOTOR	VXM1057	
						COVER S	VNL1780	
				NSP		RUBBER SHEET	VEB1272	
					55	SCREW	BBZ30P050FZK	

### 2.8 SERVO MECHANISM SECTION (2/2)



Mark	No.	. Description	Part No.	Mark	No	. Description	Part No.
NSP	1	TNMB ASSY	VWG1793	NSP	21	CNNB ASSY	VWG1792
	2	CARRIAGE MOTOR	VXM1033		22	FLEXIBLE CABLE (27P)	VDA1581
NSP	3	MOTOR PULLEY	VNL1630		23	PU FPC-A	VNP1582
	4	MOTOR HOLDER	VNL1717		24	PCB HOLDER	VNL1716
	5	SCREW	BBZ30P080FMC		25	FC GUIDE	VNE2059
	6	SCREW	BMZ26P040FMC		26	PU HOLDER	VNL1715
	7	GEAR PULLEY	VNL1662		27	SW LEVER C	VNL1714
	8	RUBBER BELT	VEB1184	NSP	28	LCSB ASSY	VWG1795
	9	HOUSING ASSY (3P)	VKP2137	NSP	29	DCSB ASSY	VWG1794
	10	LEVER SWITCH	DSK1003		30	FC ARM SPRING	VBH1272
	11	MIDDLE GEAR	VNL1720		31	FC ARM	VNL1713
	12	TURN PANEL ASSY	VXA2337		32	TILT SHAFT	VLL1175
	13	GEAR S	VNL1719		33	E RING	YE30FUC
	14	TURN CAM GEAR	VNL1718		34	WASHER	WA42D080D050
	15	SWING PLATE ASSY	VXA2289		35	WASHER	WT26D070D050
	16	TURN LEVER ASSY	VXA2292		36	SCREW	PMA26P060FMC
	17	TURN PLATE ASSY	VXA2290		37	CUSHION	VEC1917
	18	PU FPC-B	VNP1583		38	TUBE	VEB1273
	19	FLEXIBLE CABLE (26P)	VDA1580		39	BINDER	Z09-056
	20	CONNECTOR ASSY	PG02KK-E10				

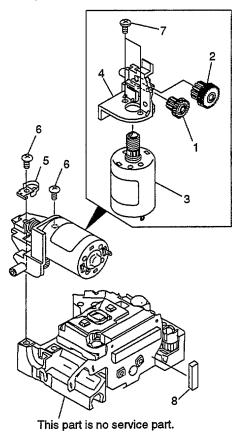
#### 2.9 DVD CARRIAGE ASSY



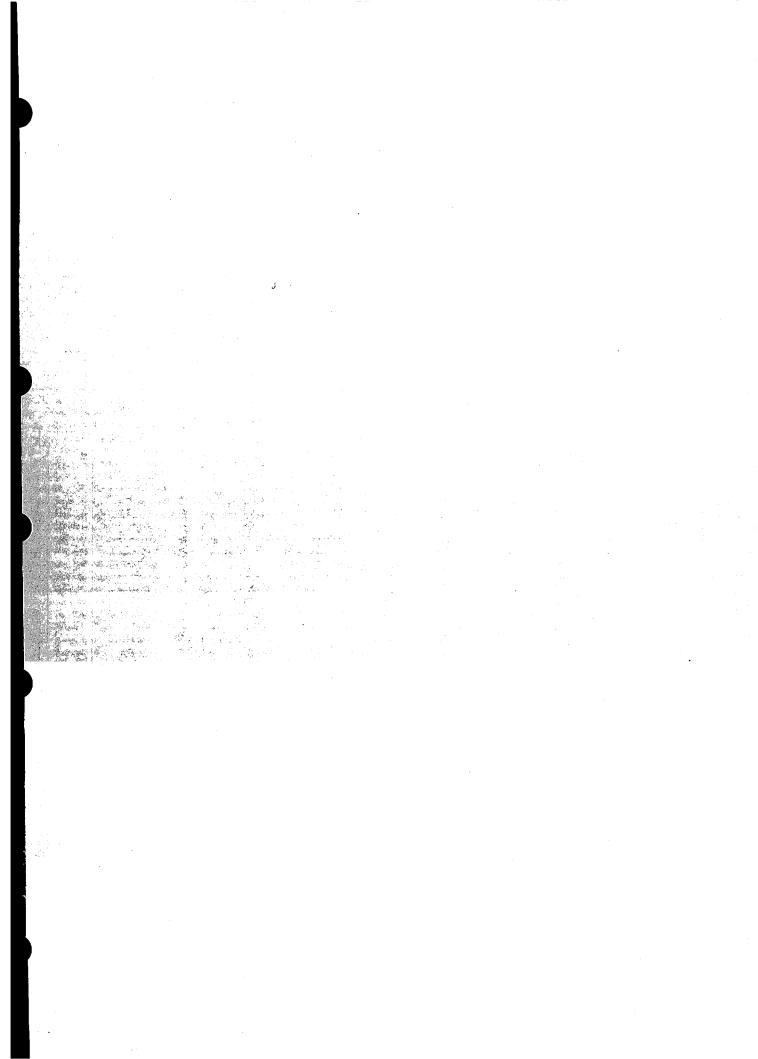
#### **Parts List**

Mark	No	. Description	Part No.		
	1	CA GEAR(A)	VNL1782		
	2	CA GEAR B ASSY	VXX2471		
	3	SLIDER MOTOR ASSY	VXX2472		
	4	MOTOR HOLDER	VNL1779		
	5	THRUST HOLDER	VBK1058		
	6	CA GUIDE B	VNL1721		
	7	SCREW	BBZ20P050FZK		
	8	SCREW	PMZ20P030FMC		

#### 2.10 CLD CARRIAGE ASSY

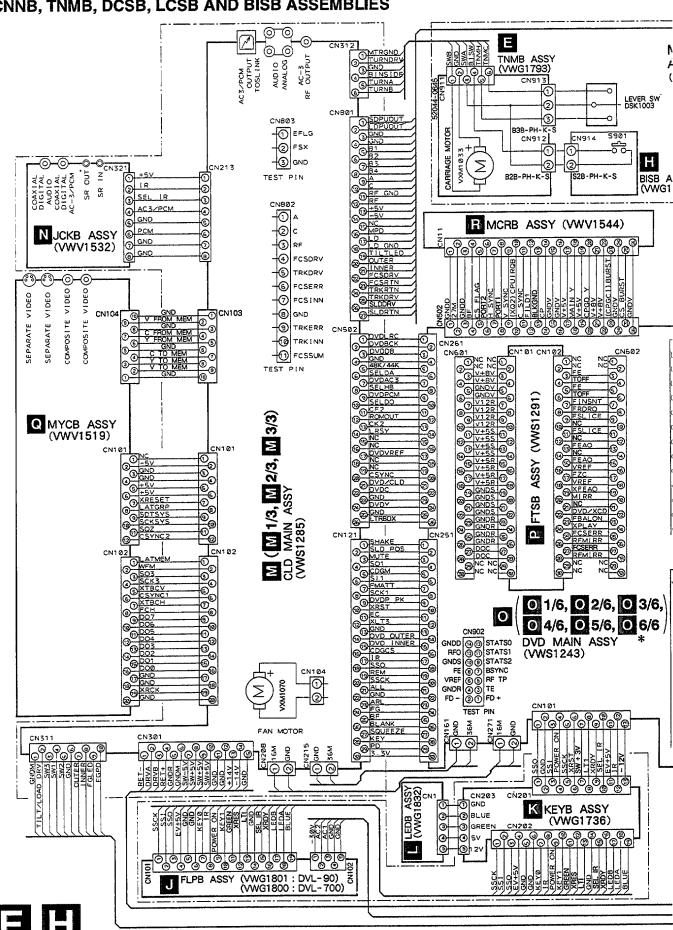


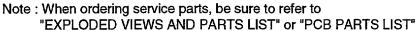
Mark	No.	Description	Part No.
	1	CA GEAR(A)	VNL1782
	2	CA GEAR(B)	VNL1639
	3	SLIDER MOTOR ASSY	VXX2472
	4	MOTOR HOLDER	VNL1779
	5	THRUST HOLDER	VBK1058
	6	SCREW	PBZ20P050FMC
	7	SCREW	PMZ20P030FMC
	8	CUSHION B	VEC1931

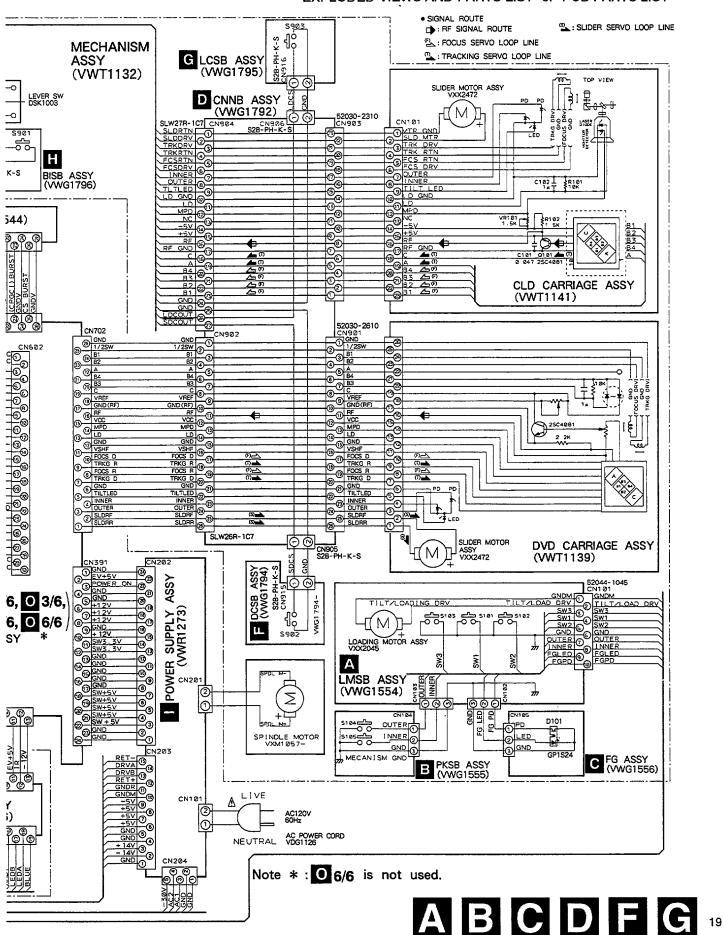


#### 3. SCHEMATIC DIAGRAM

3.1 OVERALL WIRING DIAGRAM, LMSB, PKSB, FG, CNNB, TNMB, DCSB, LCSB AND BISB ASSEMBLIES





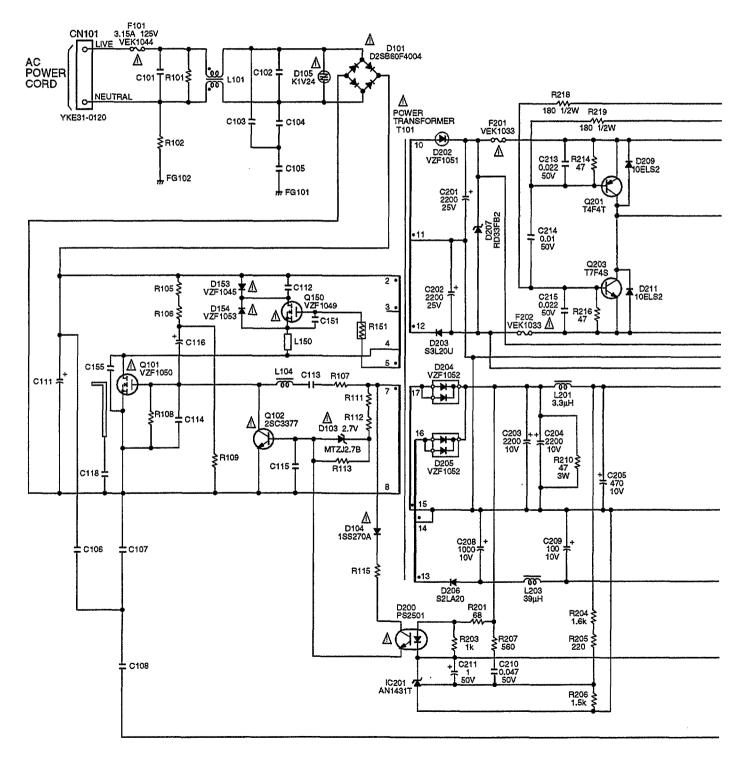


#### 3.2 POWER SUPPLY ASSY

• NOTE FOR FUSE REPLACEMENT

CAUTION -FOR CONTINUED PROTECTION AGAINST RISK OF FIRE.
REPLACE ONLY WITH SAME TYPE AND RATINGS ONLY.

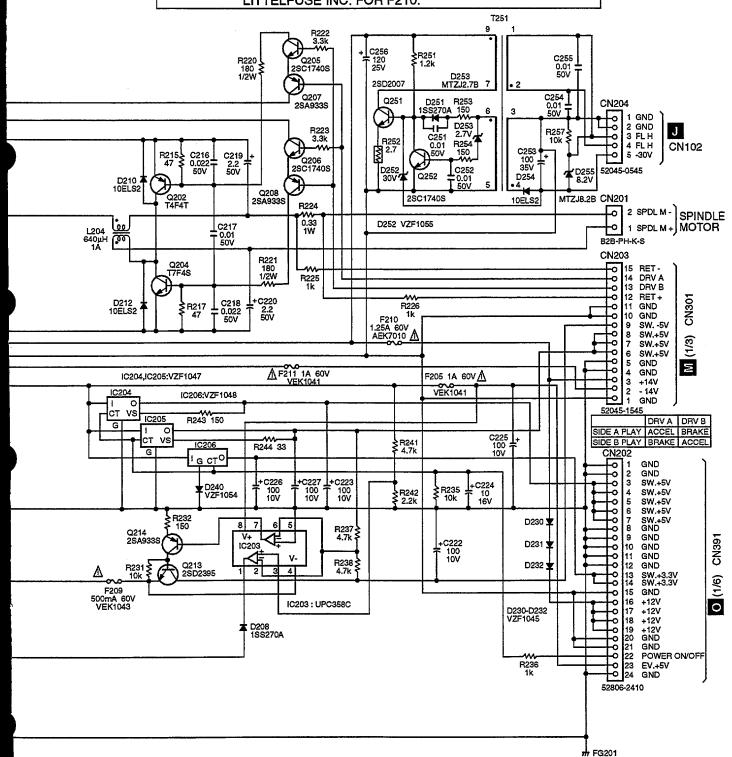
POWER SUPPLY ASSY (VWR1273)



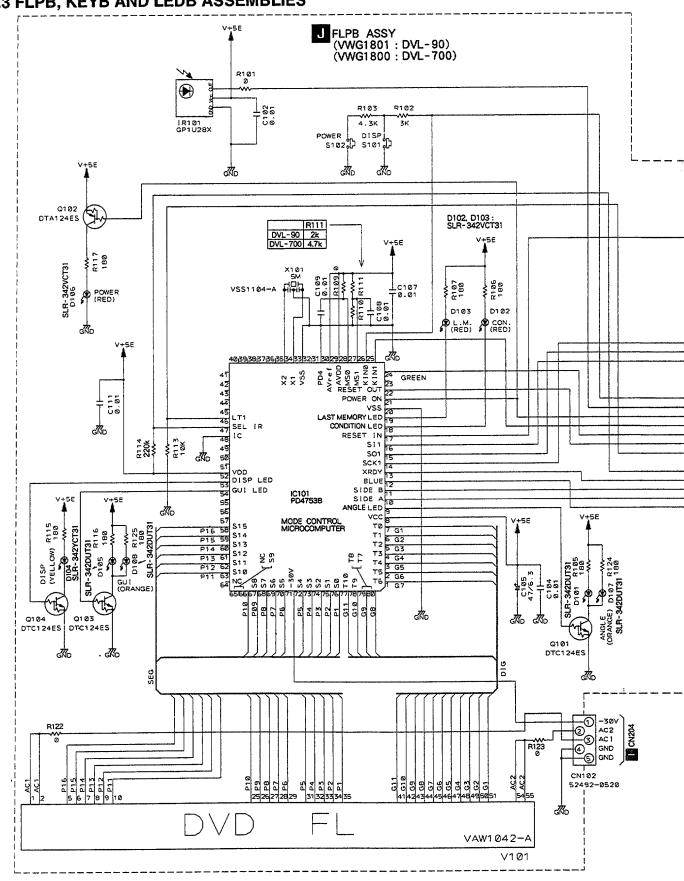
#### « NOTE OF SPARE PARTS IN POWER SUPPLY (SYPS) ASSY »

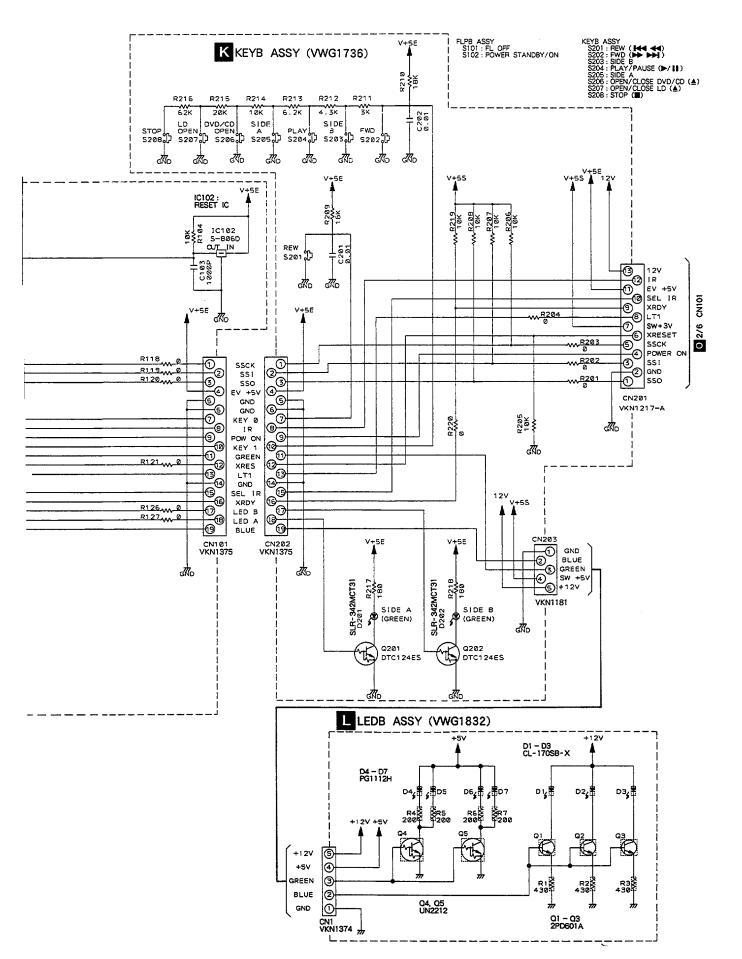
- In case of repairing, use the described parts only to prevent an accident.
- Please write the red ✓ mark on the board when the primary section of POWER SUPPLY (SYPS) Assy is repaired.
- Please take care to keep the space, not touching other parts when replacing the parts.

CAUTION -FOR CONTINUED PROTECTION AGAINST RISK OF FIRE.
REPLACE ONLY WITH SAME TYPE NO. 491001 MFD.
BY LITTELFUSE INC. FOR F205 AND F211, 491.500 MFD.
BY LITTELFUSE INC. FOR F209, 4911.25 MFD. BY
LITTELFUSE INC. FOR F210.

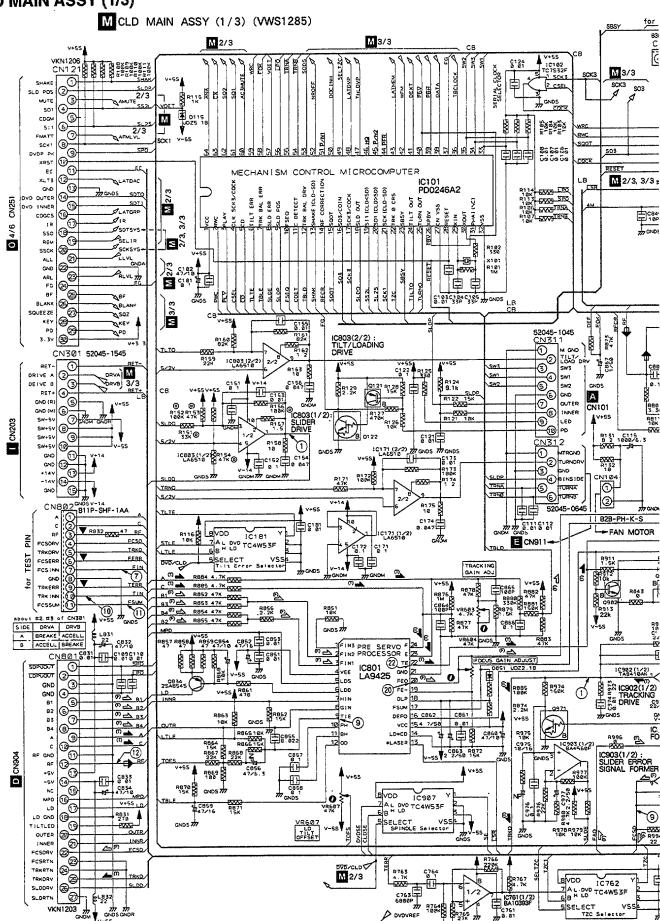


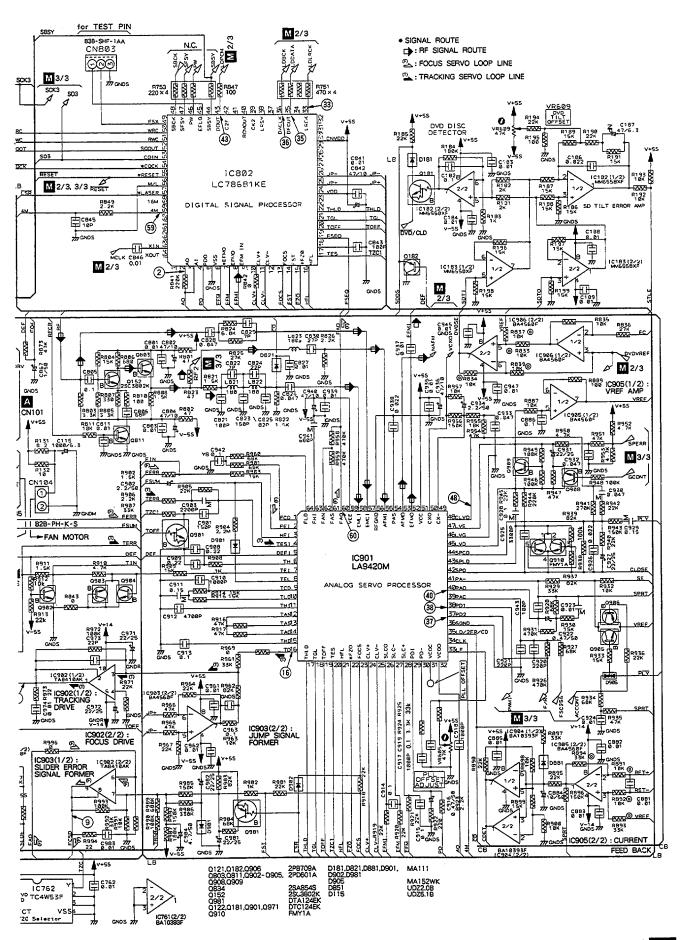
#### 3.3 FLPB, KEYB AND LEDB ASSEMBLIES



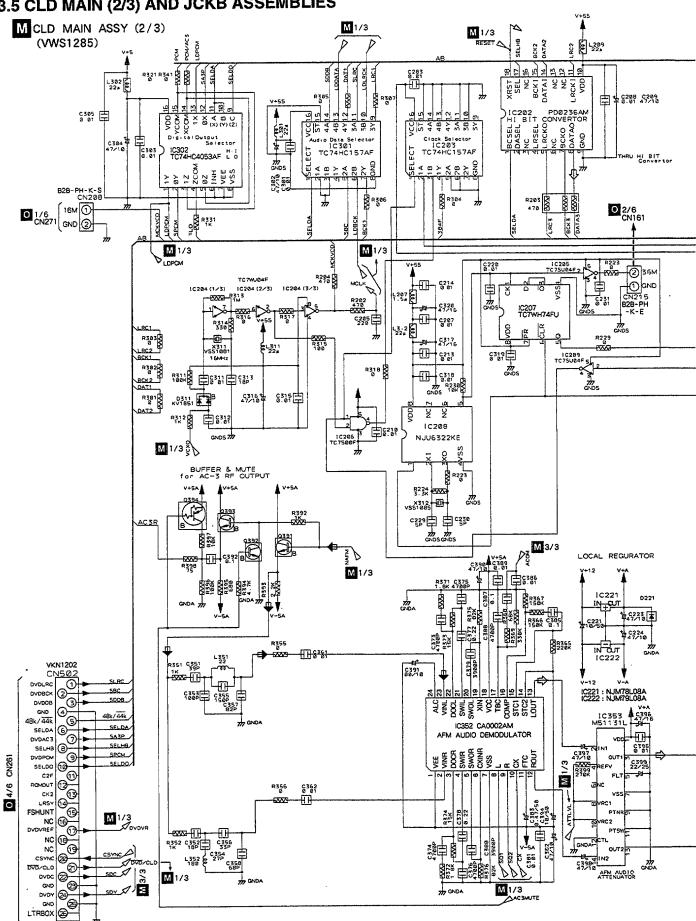


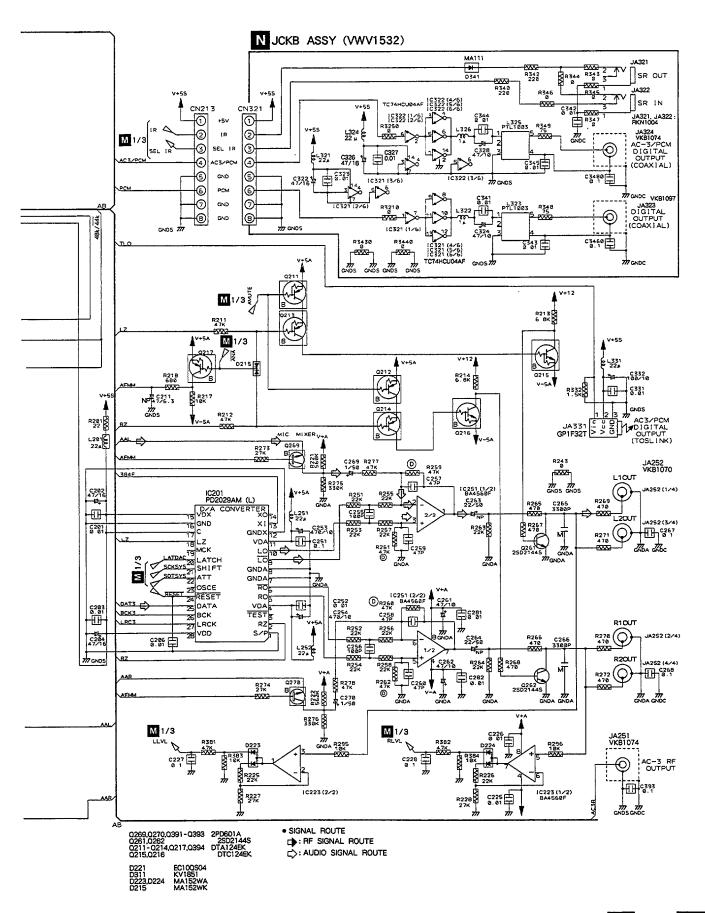
#### 3.4 CLD MAIN ASSY (1/3)



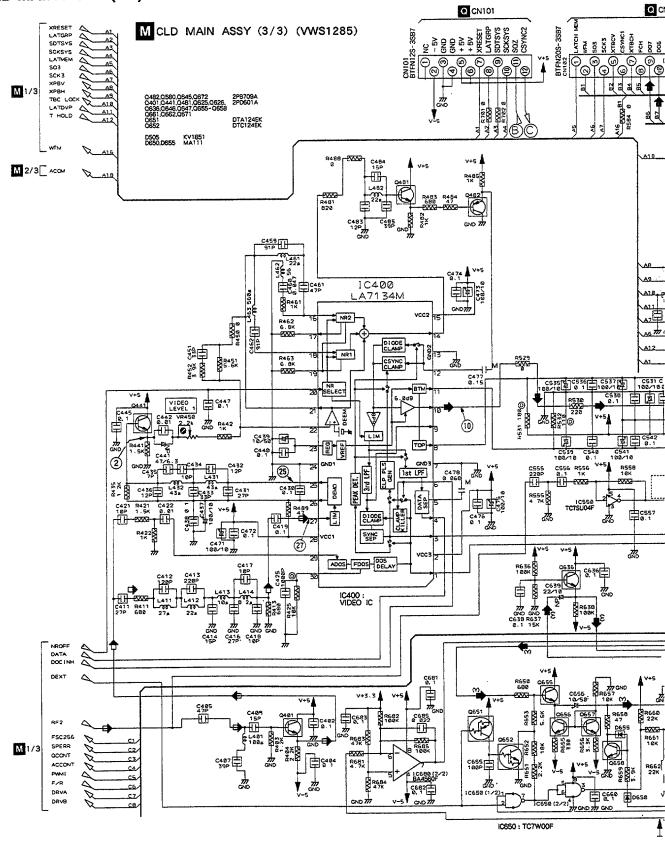


#### 3.5 CLD MAIN (2/3) AND JCKB ASSEMBLIES

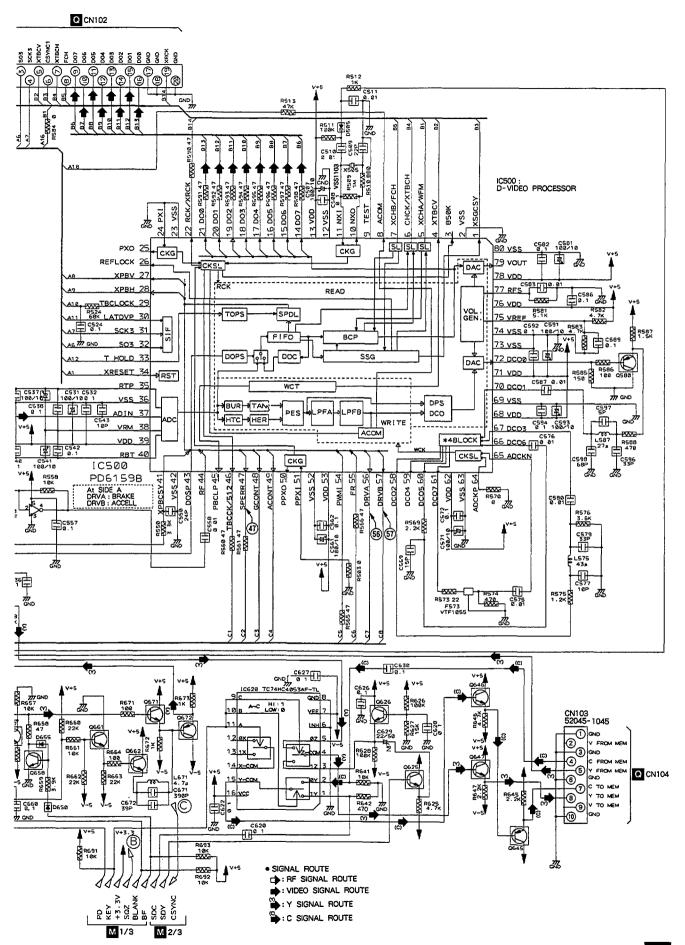


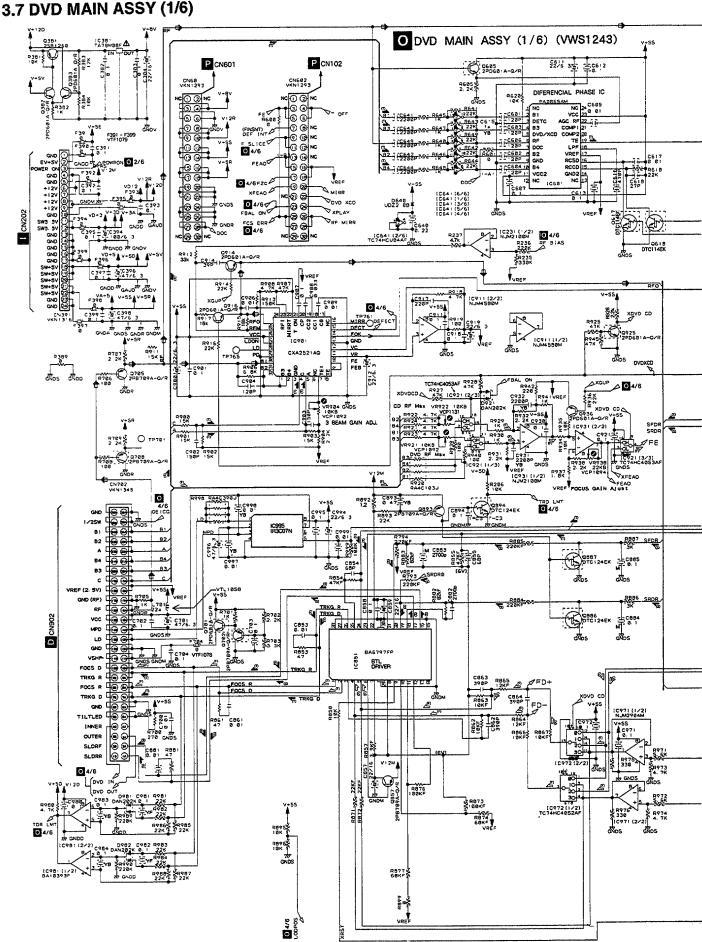


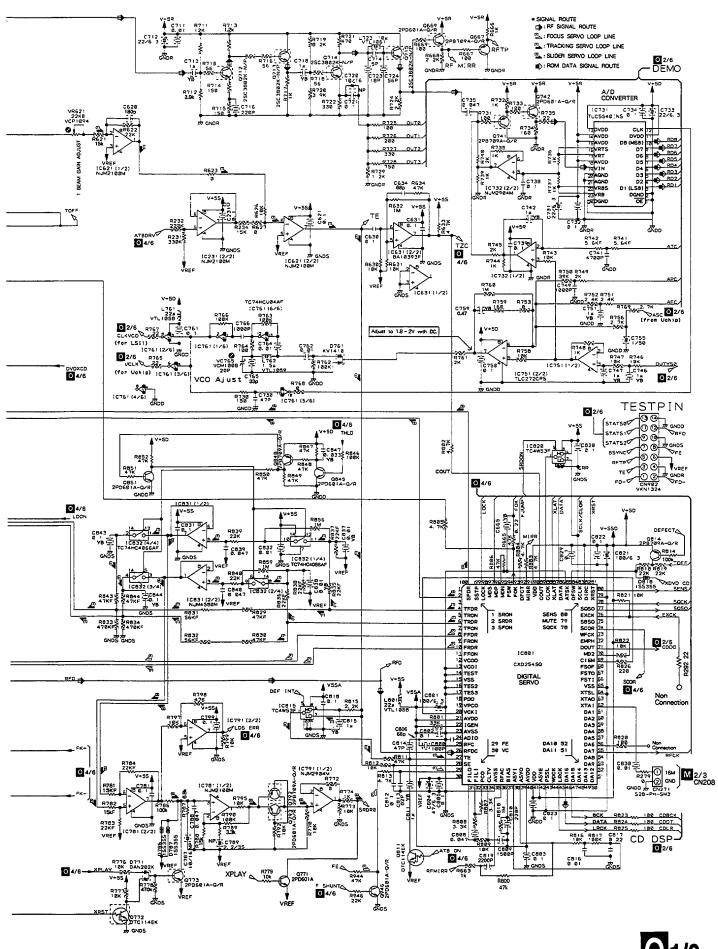
#### 3.6 CLD MAIN ASSY (3/3)



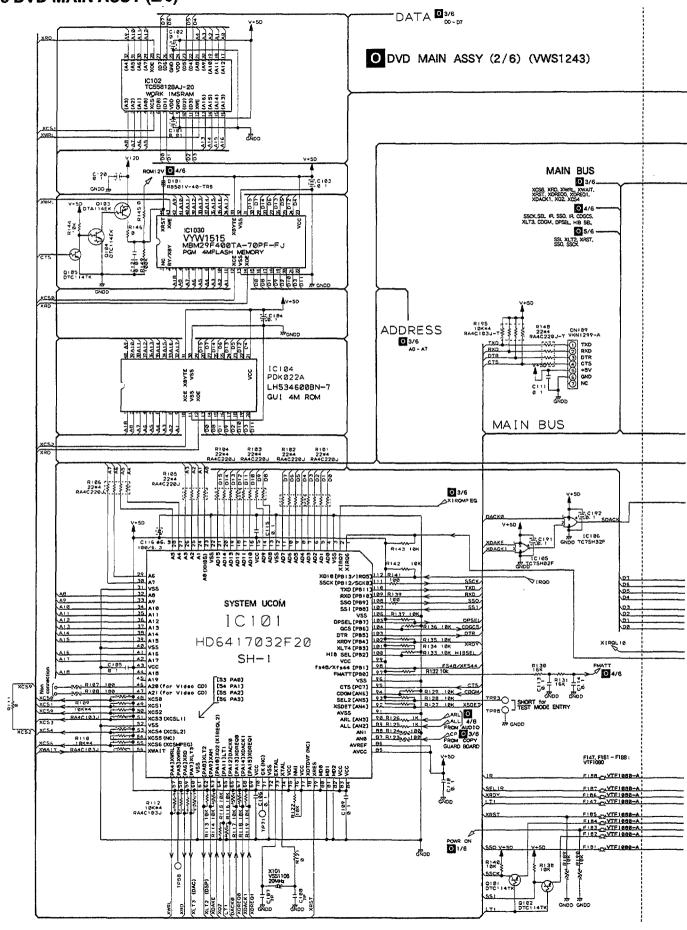


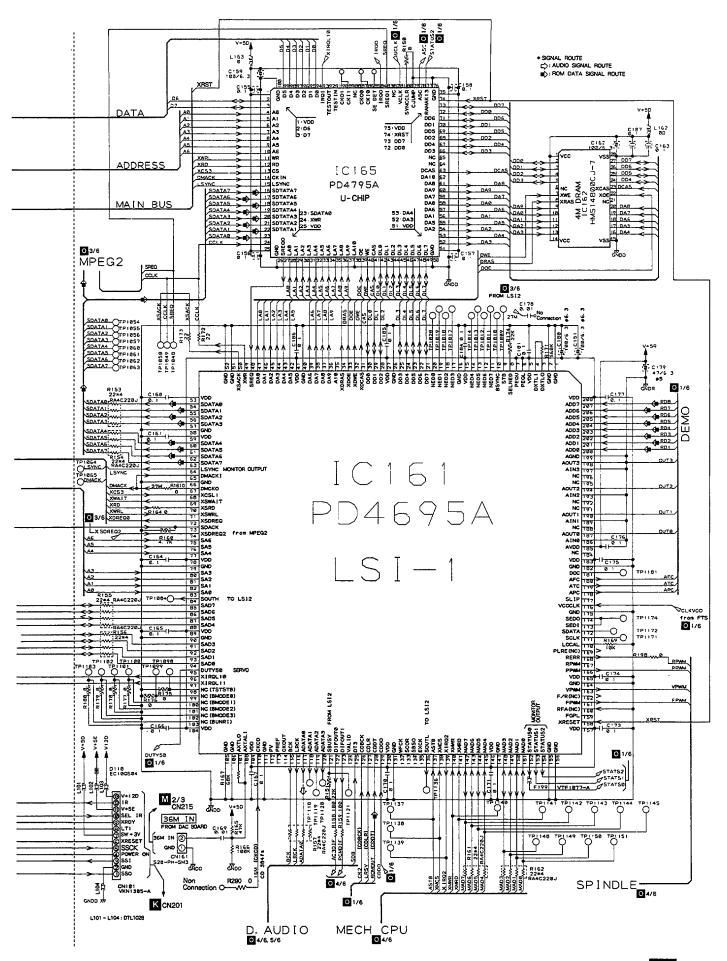


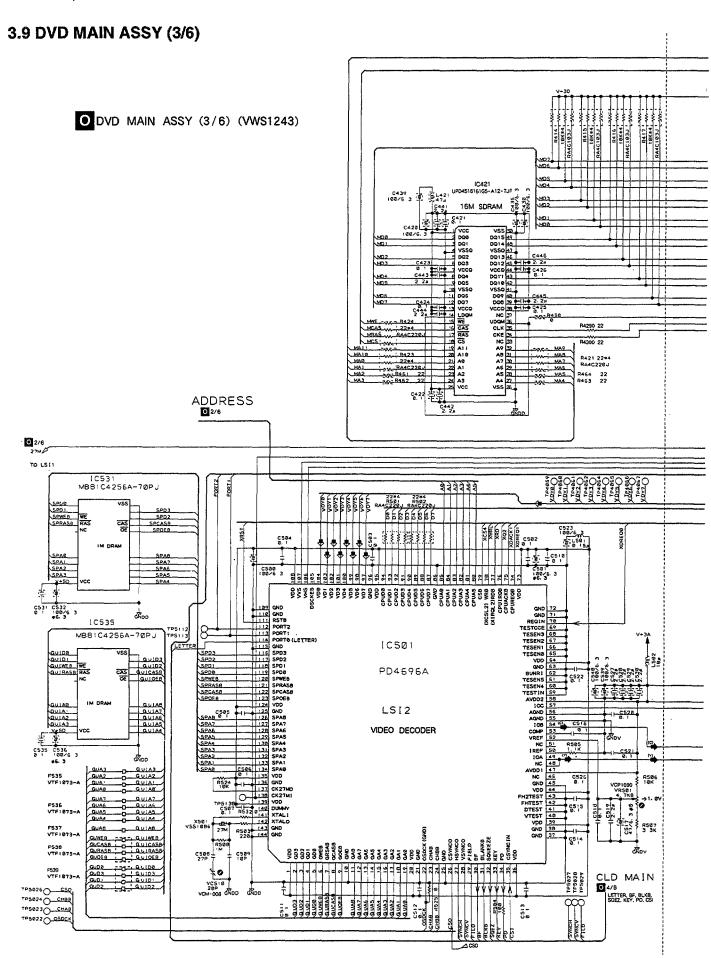


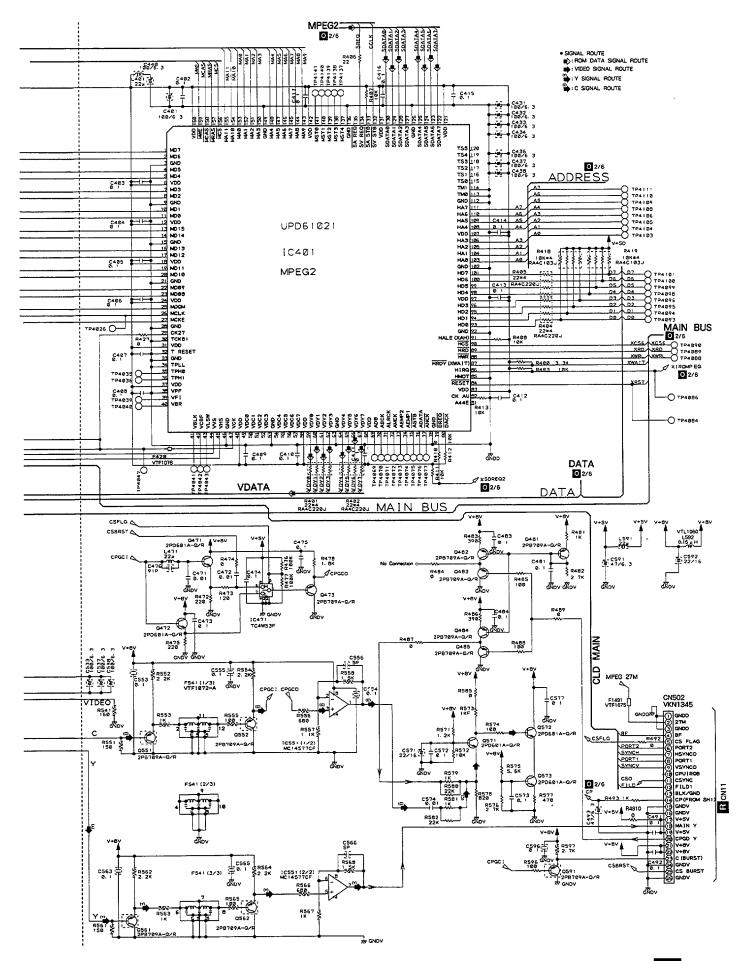


#### **3.8 DVD MAIN ASSY (2/6)**

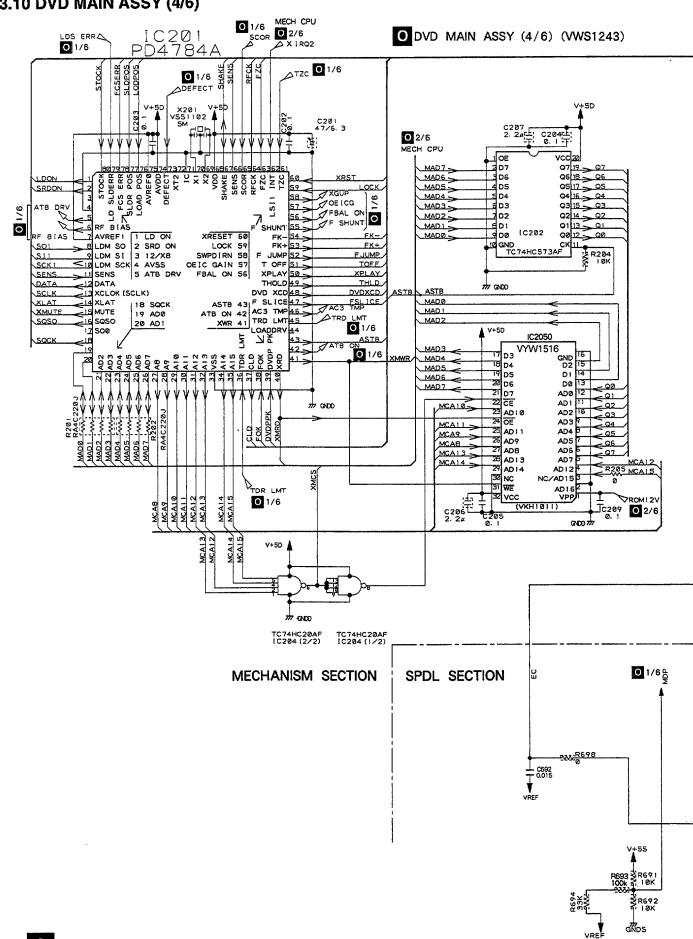


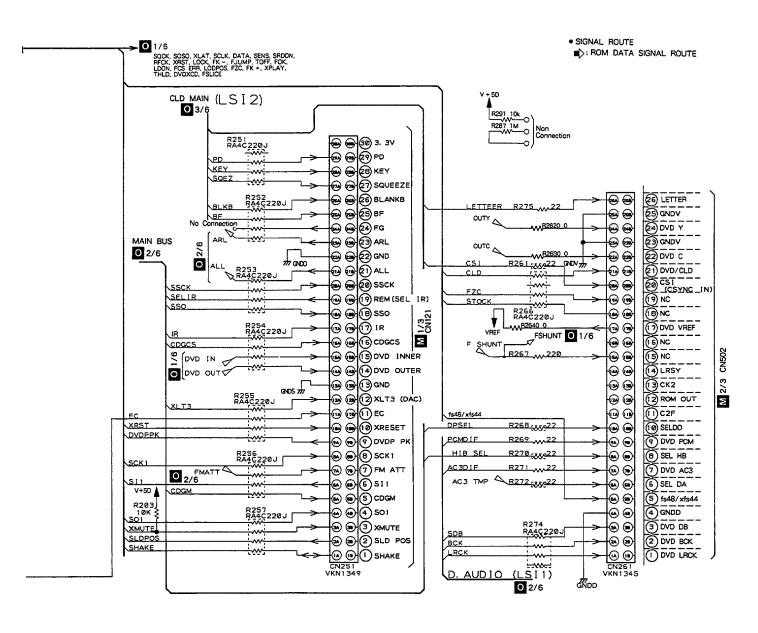






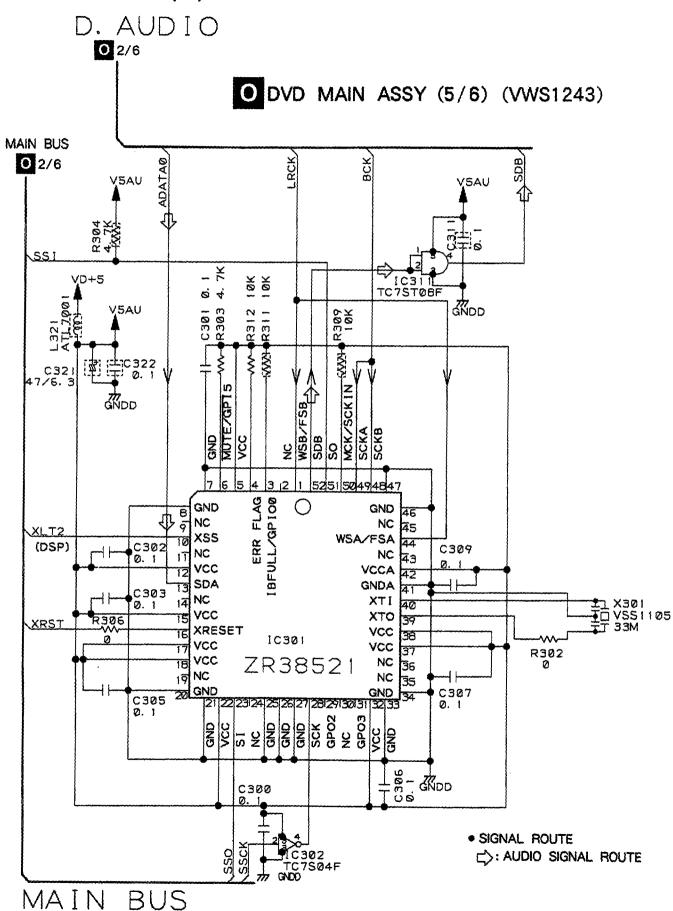
#### 3.10 DVD MAIN ASSY (4/6)





SPDL 0 2/6 ∑; C681 470p R681 200k R680 200k C677 8200P FPWM R677 68K 100 V+5S R676 R675 R661 200k R690 R672 3k C676 T 0. 01 R673 10k R689 R682 ≸ \$R662 47K R688 GNDS IC571 (1/2) NJM2904M R674 IC672 (2/2)77 NJM2904M GNDS VREF VREF

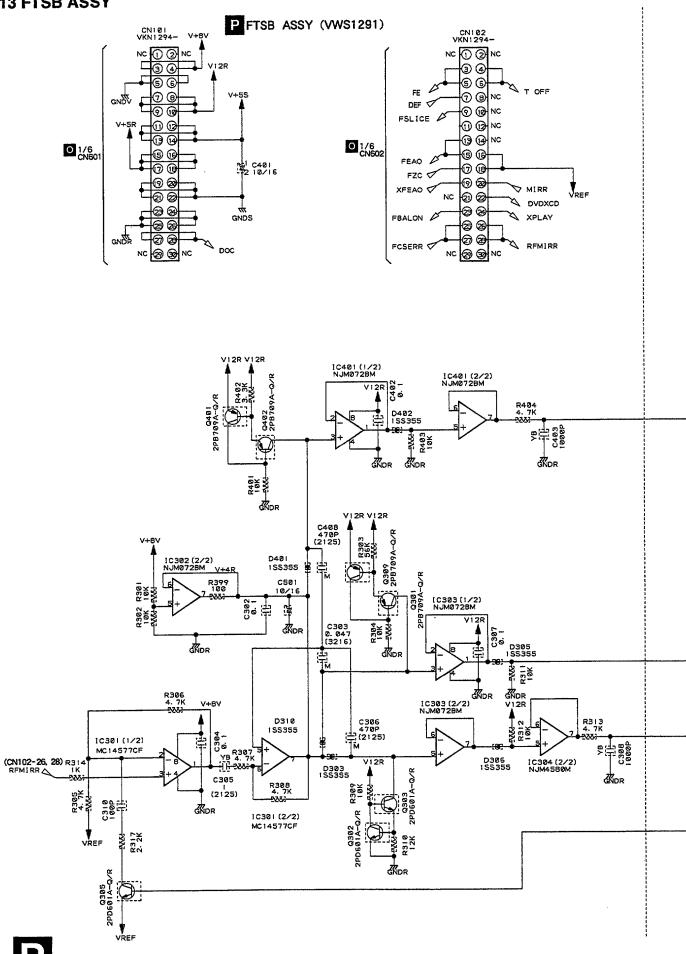
# 3.11 DVD MAIN ASSY (5/6)

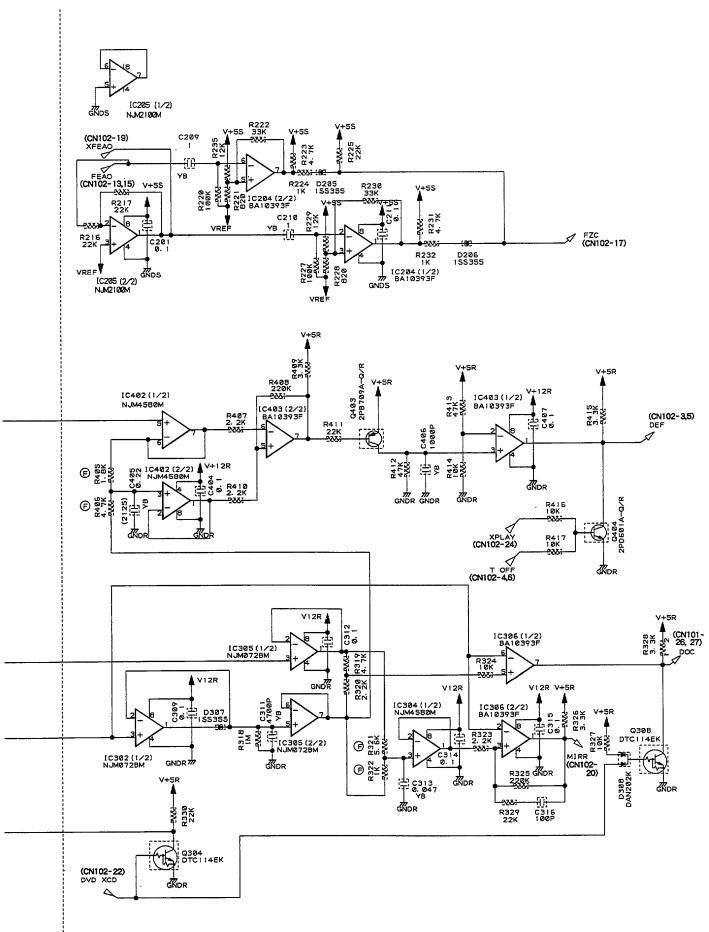


3.12 DVD MAIN ASSY (6/6)

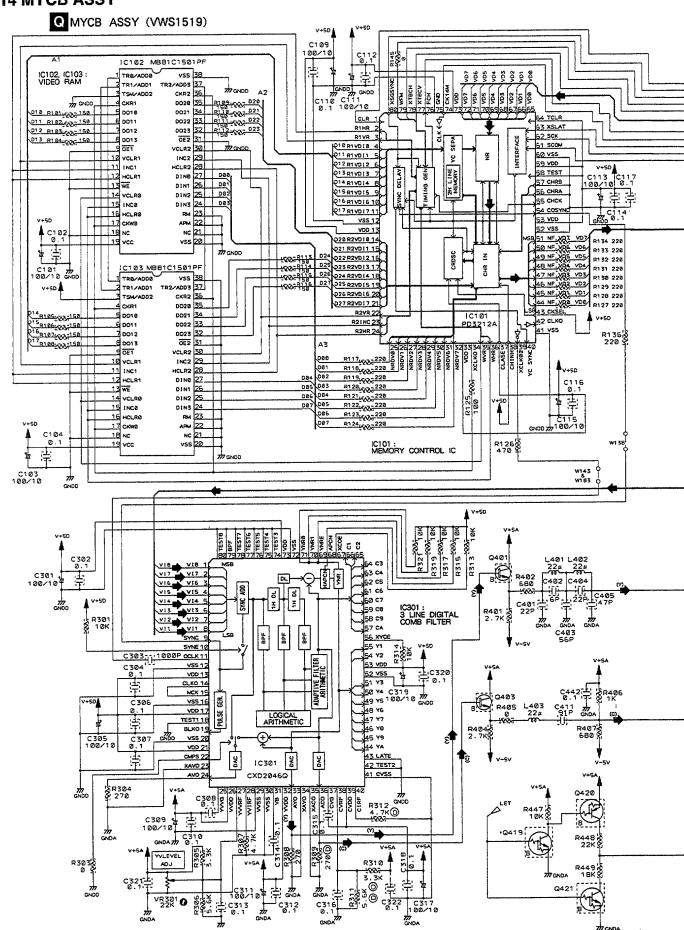
06/6 DVD MAIN ASSY (6/6) (VIDEO CD SECTION) is not used on this model.

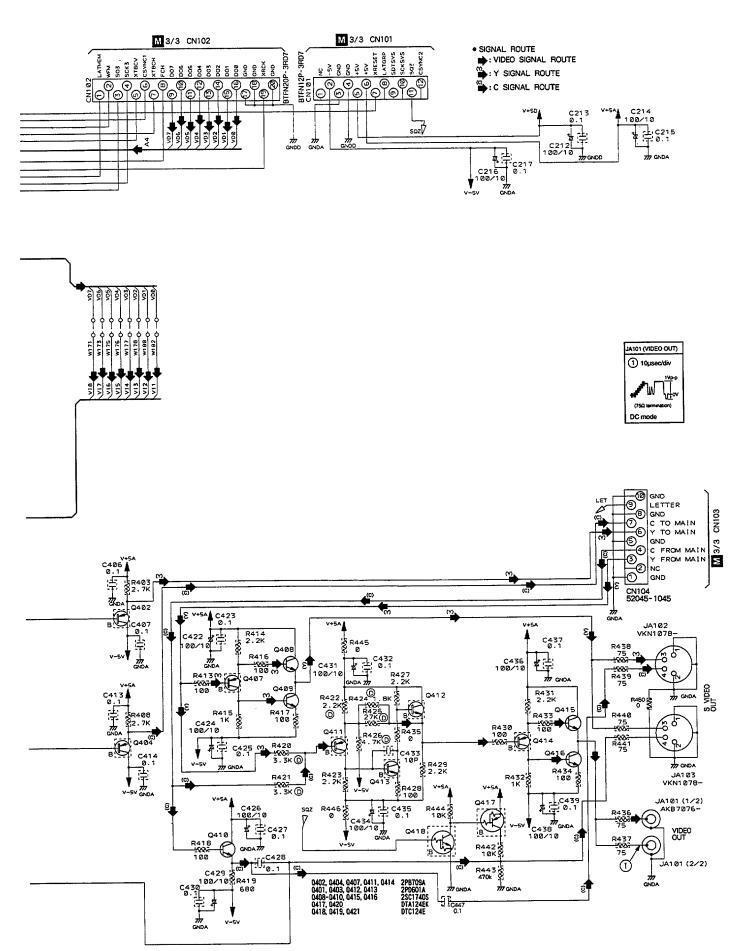
#### 3.13 FTSB ASSY



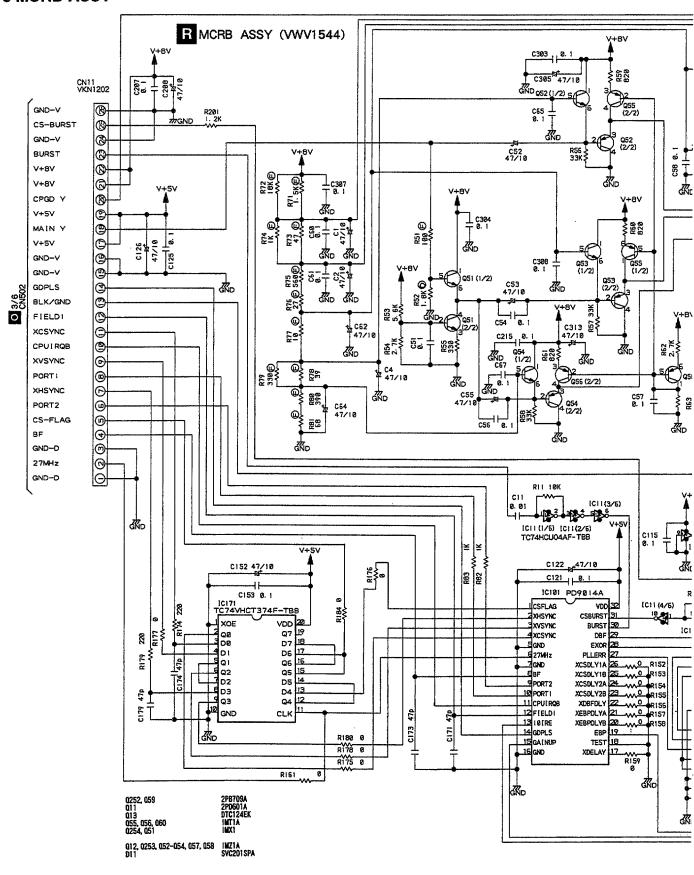


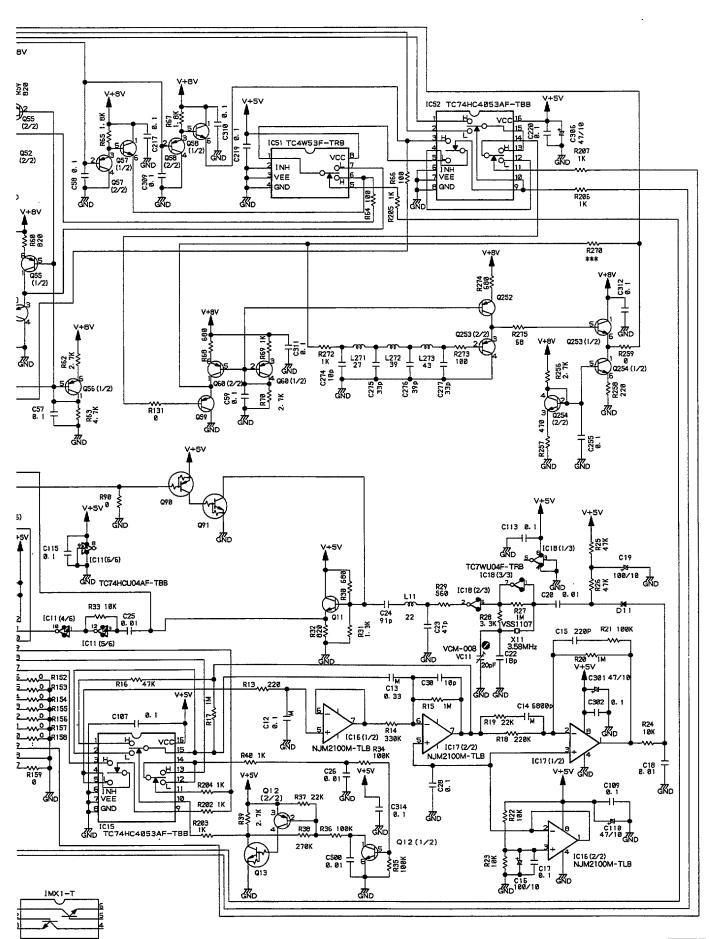
#### 3.14 MYCB ASSY





#### 3.15 MCRB ASSY



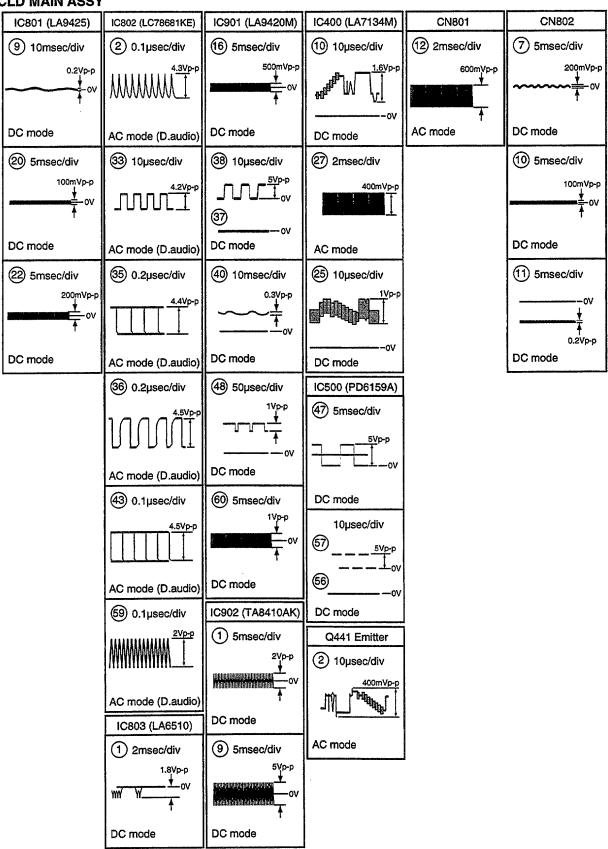


#### WAVEFORMS AND VOLTAGE

Note: (No) in the table correspond to the pin number.

Measurement condition: In case when (D.audio) is written, at time when disc that has digital audio recording is played.

# M CLD MAIN ASSY



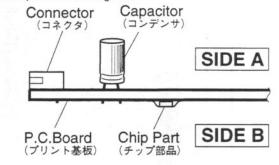
# 4. PCB CONNECTION DIAGRAM

#### **NOTE FOR PCB DIAGRAMS:**

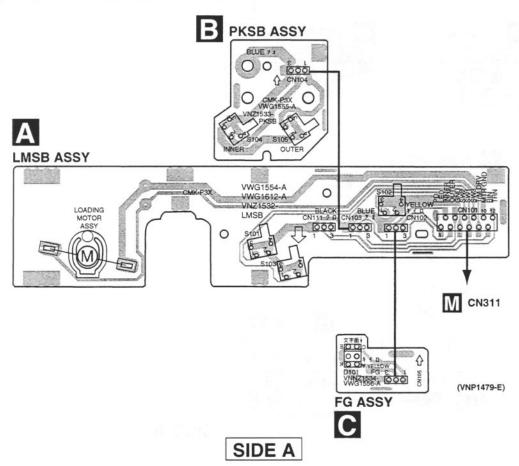
- 1. Part numbers in PCB diagrams match those in the schematic diagrams.
- 2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name
000 B C E		Transistor
●	BCEBCE	Transistor with resistor
000 DGS		Field effect transistor
@00000X	******	Resistor array
000		3-terminal regulator

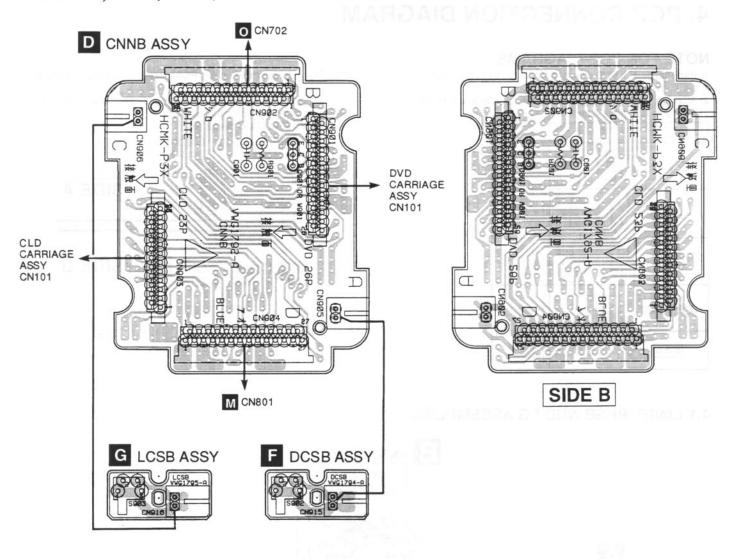
- 3. The parts mounted on this PCB include all necessary parts for several destinations.
- For further information for respective destinations, be sure to check with the schematic diagram.
- 4. View point of PCB diagrams.

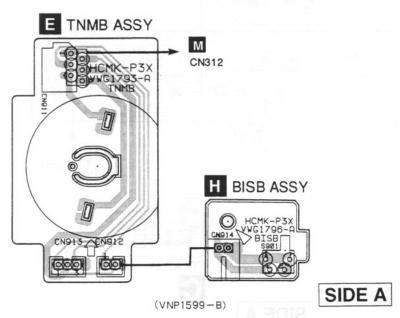


#### 4.1 LMSB, PKSB AND FG ASSEMBLIES

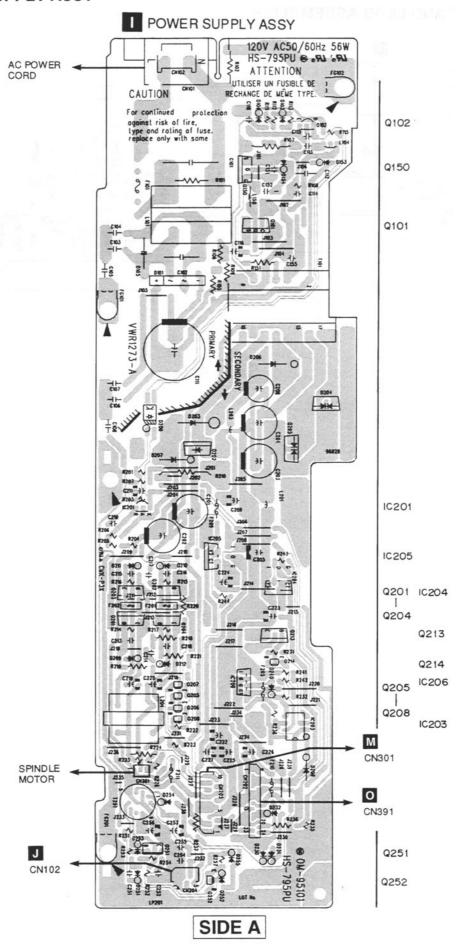


#### 4.2 CNNB, TNMB, DCSB, LCSB AND BISB ASSEMBLIES



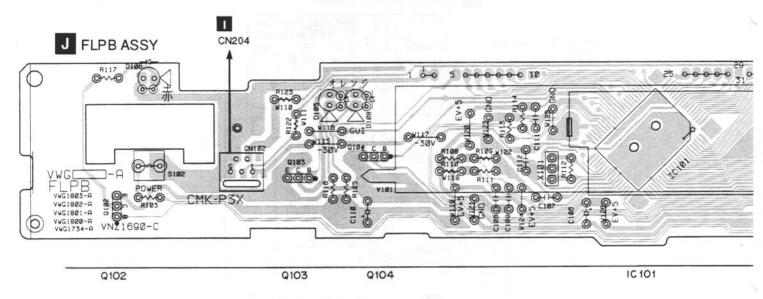


#### **4.3 POWER SUPPLY ASSY**

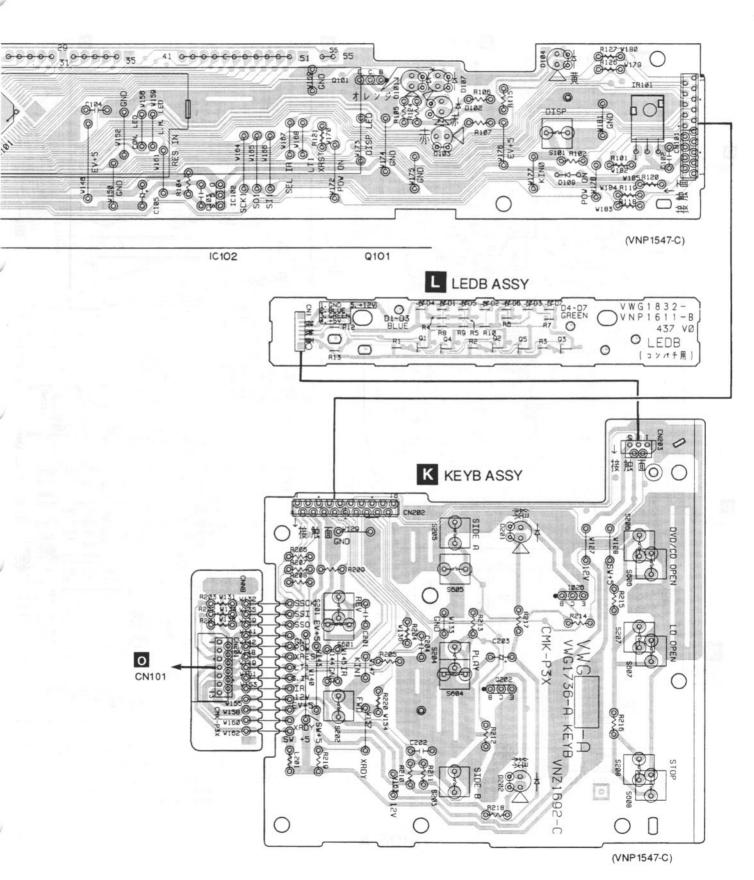


# **DVL-90, DVL-700**

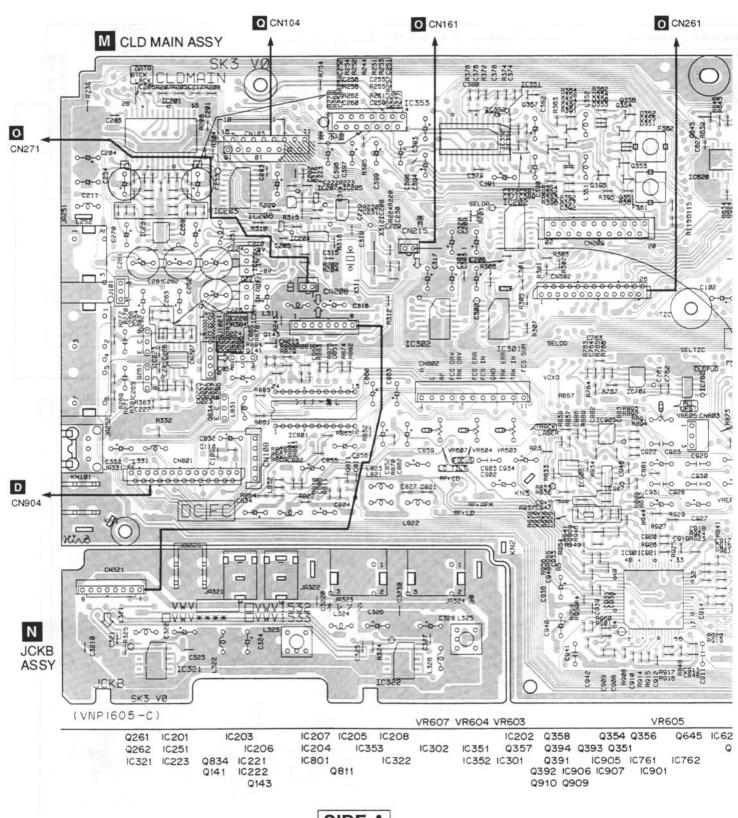
## 4.4 FLPB, KEYB AND LEDB ASSEMBLIES



SIDE A

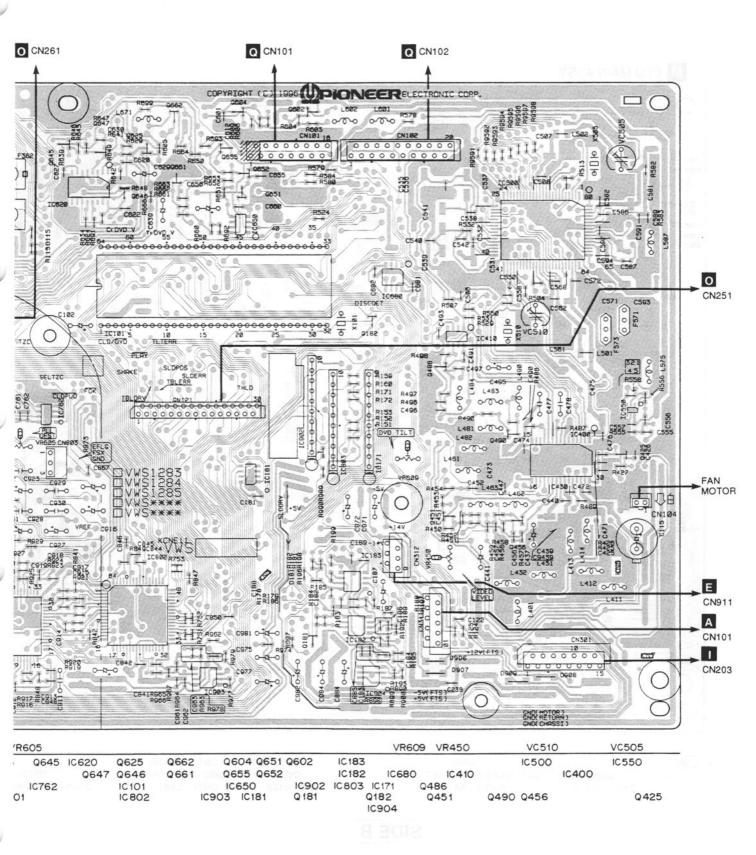


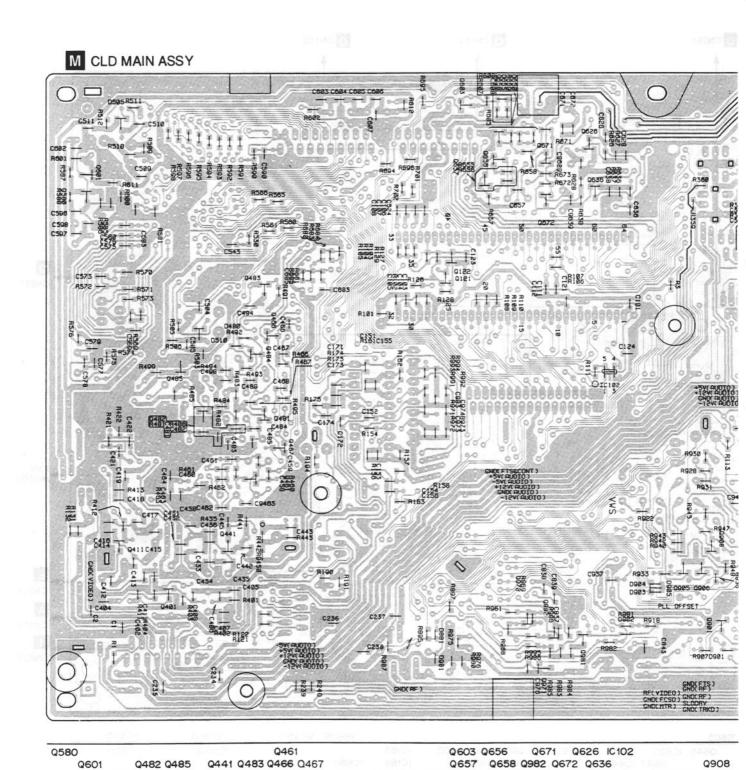
#### 4.5 CLD MAIN AND JCKB ASSEMBLIES











SIDE B

Q121 Q122

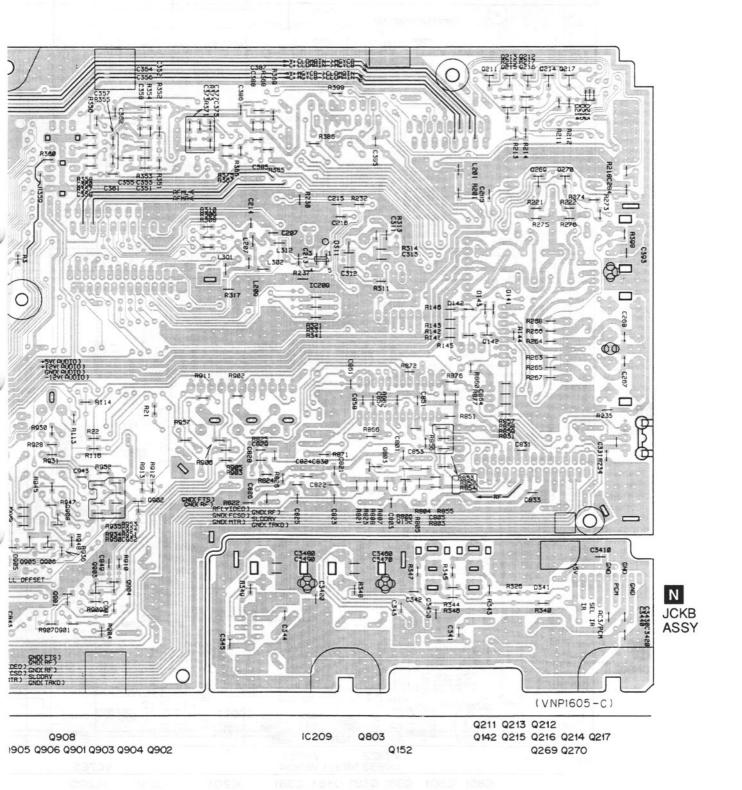
Q972 Q971 Q981

Q905 Q906 Q90°

Q484 Q481

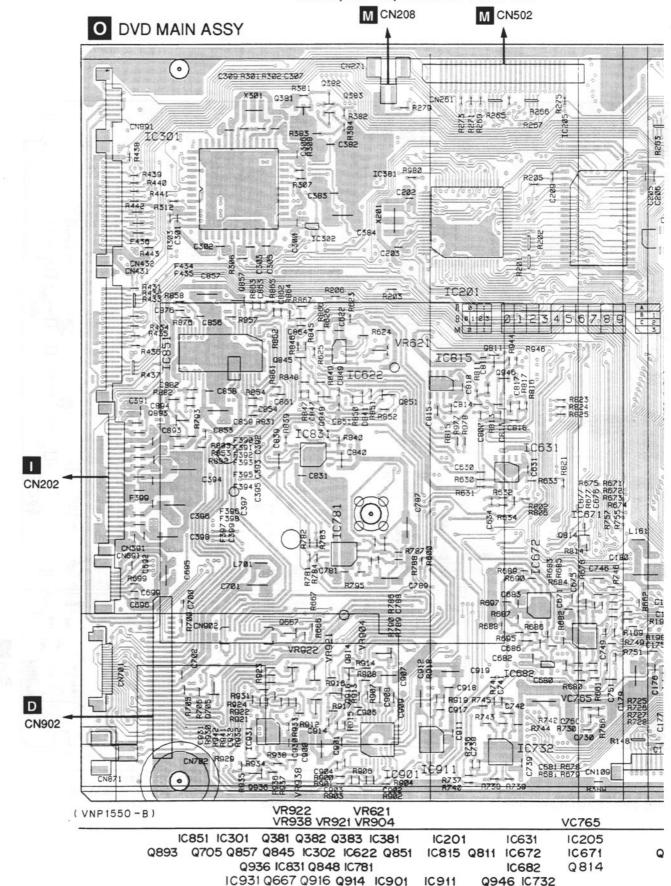
Q411

Q401



#### 4.6 DVD MAIN ASSY

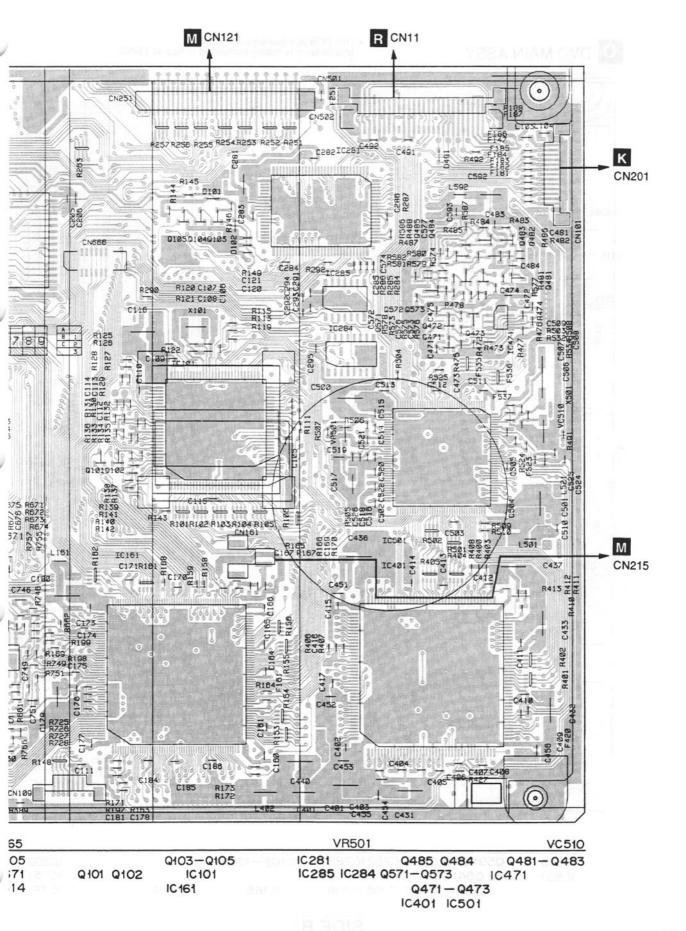
. This PCB is a four-layered board. Middle layer is mainly connected to Vcc and GND.

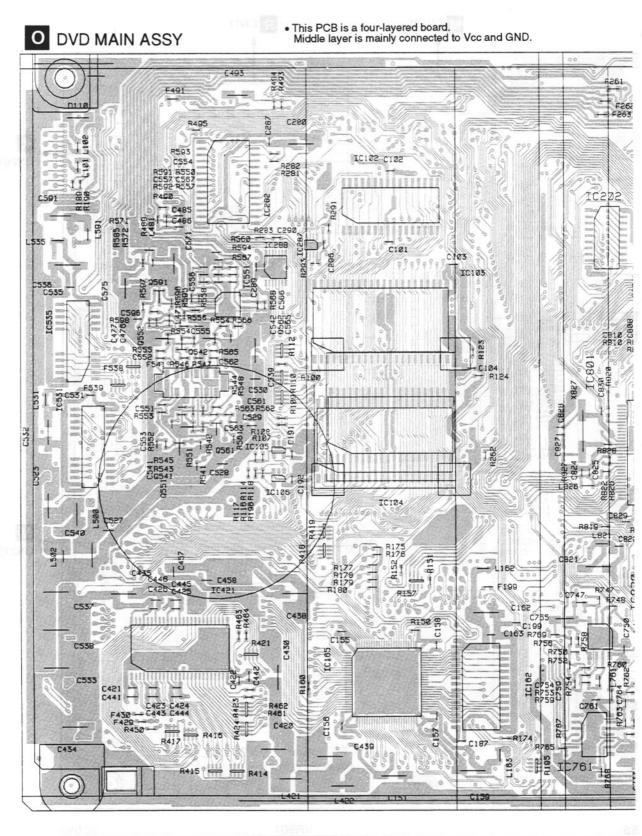


SIDE A

IC911

Q946 IC732



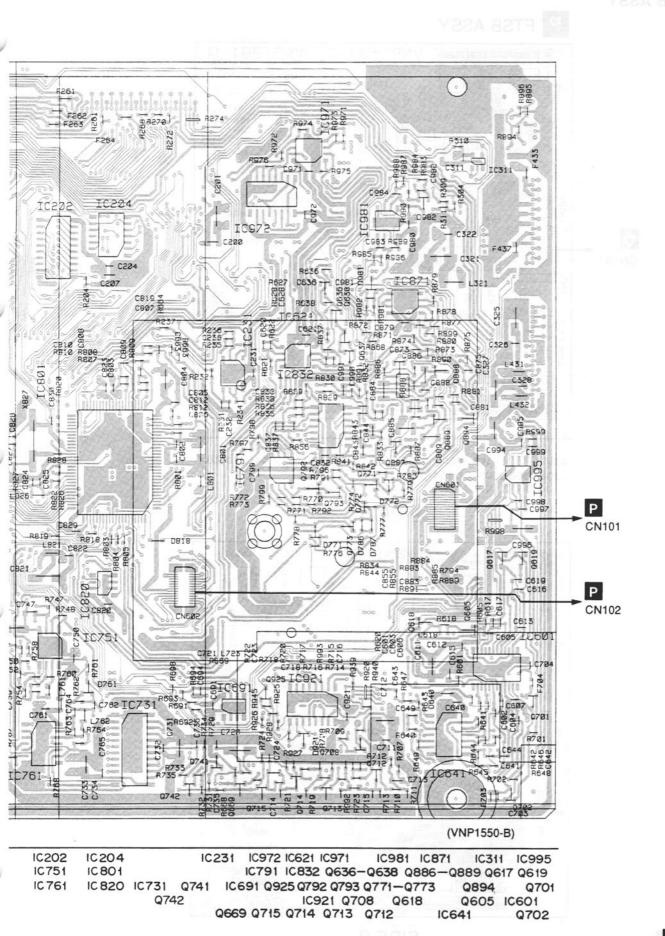


 IC535
 Q591 Q542Q562 IC282 IC288
 IC102 — IC104
 IC202

 IC531
 Q552 Q541 Q561 IC551
 IC287
 IC751

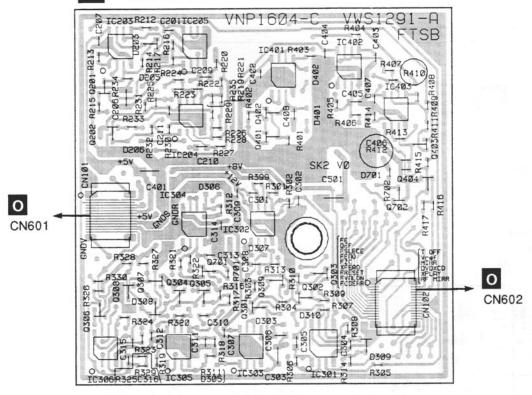
 Q551 IC421
 IC105 IC106
 IC165
 IC162
 IC761

SIDE B

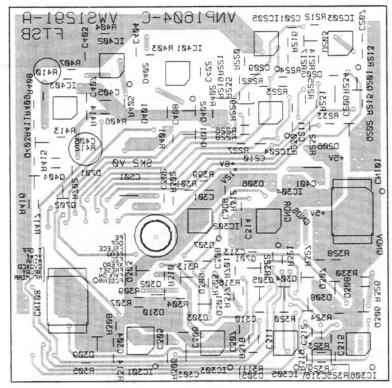


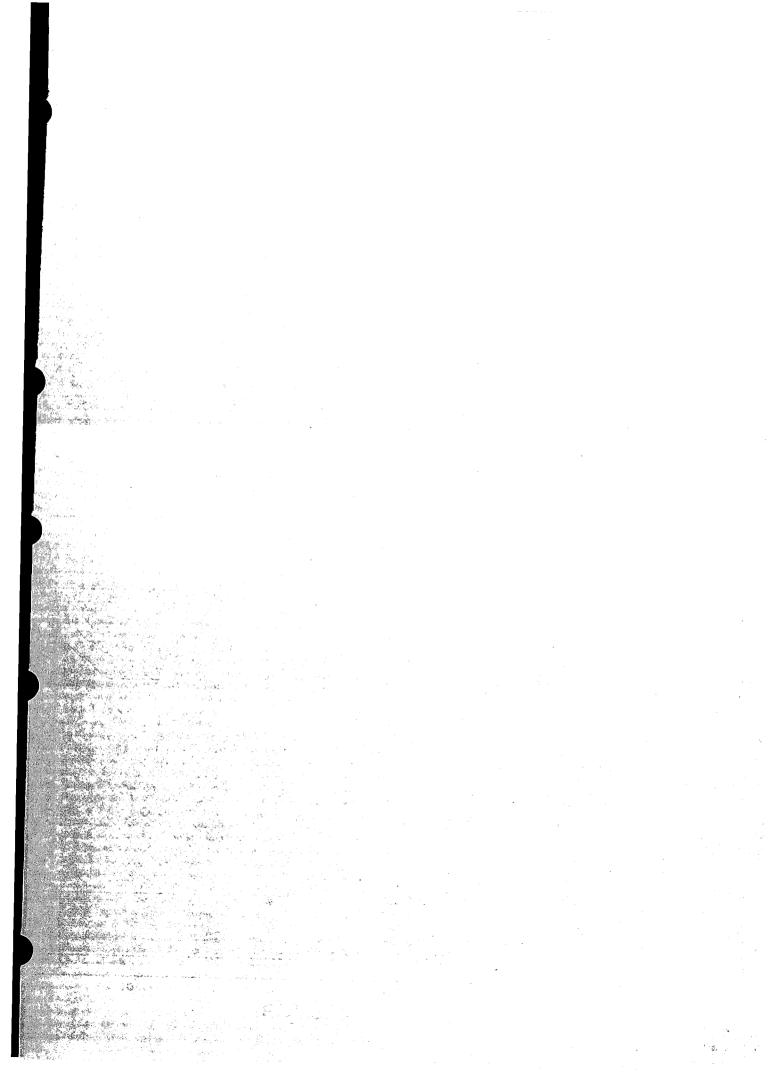
#### 4.7 FTSB ASSY

# P FTSB ASSY

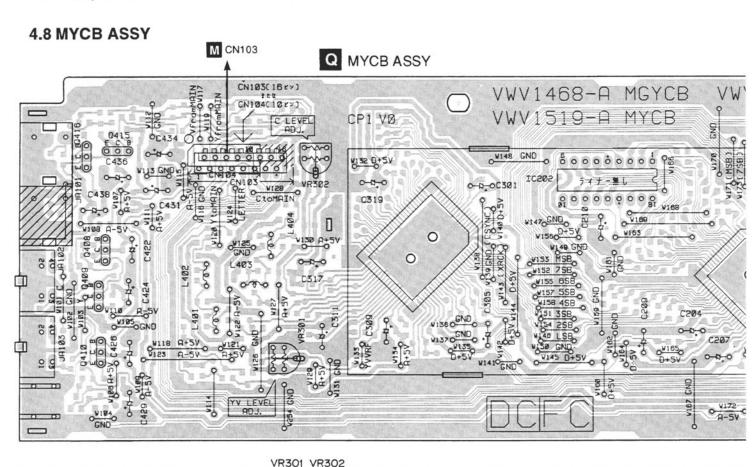


# SIDE A





#### **DVL-90, DVL-700**

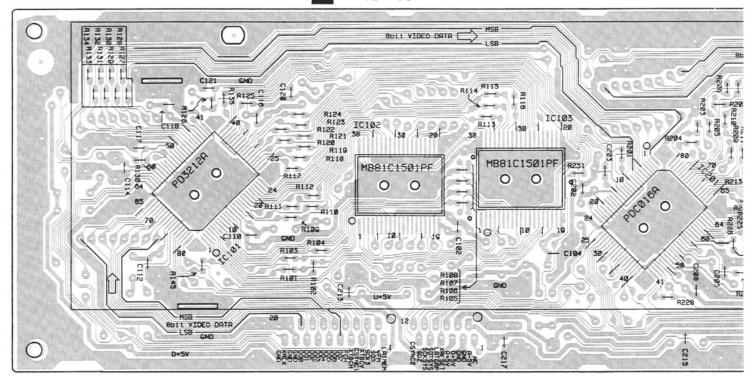


Q416 Q415 Q408-Q410

SIDE A

IC202

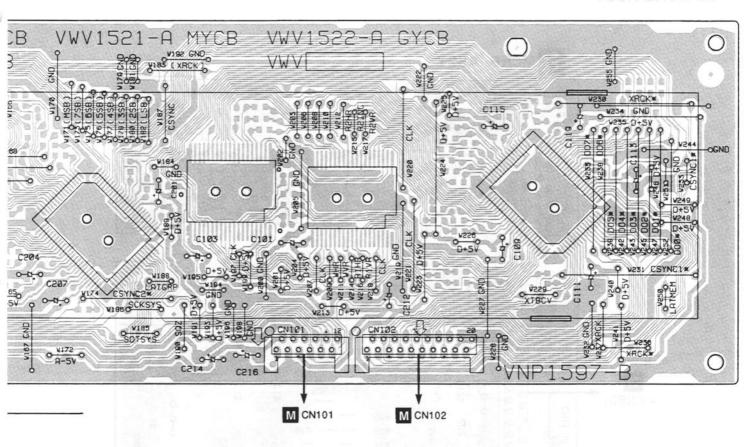
# Q MYCB ASSY

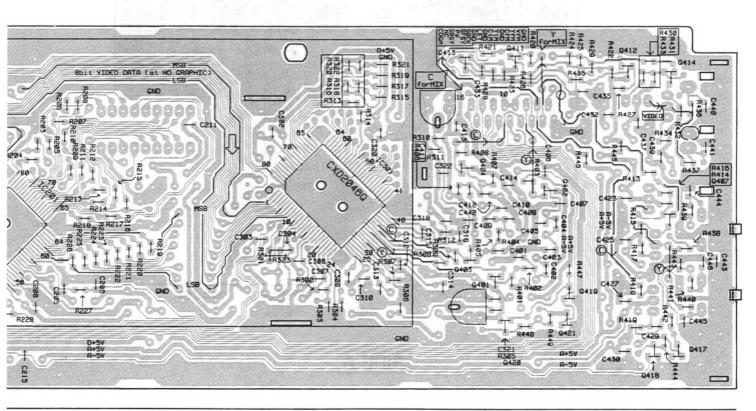


IC101 IC102 IC103 IC201



4.9 MCRB ASSY



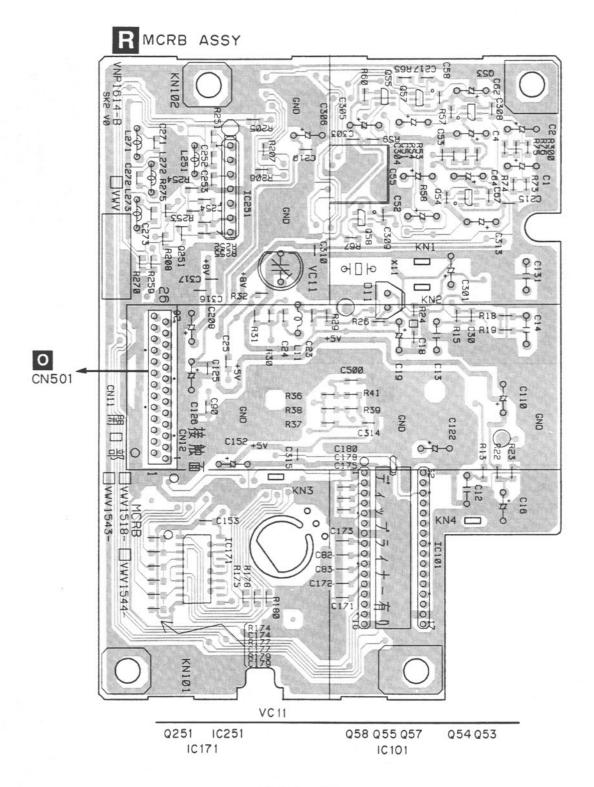


IC301

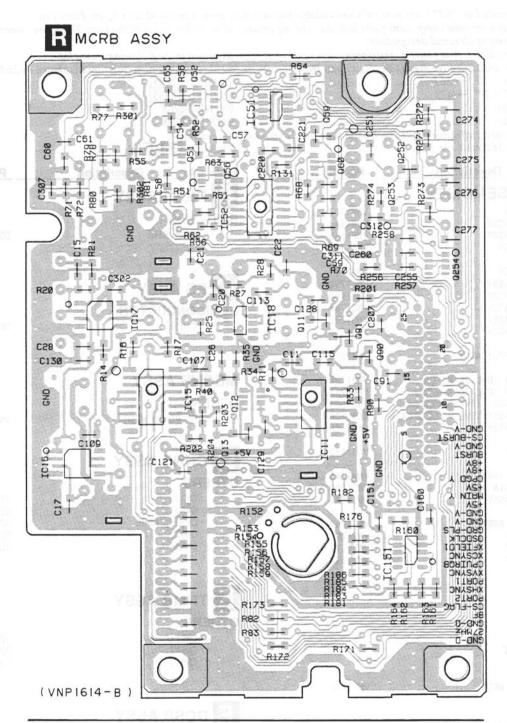
Q413 Q404 Q411 Q402 Q403 Q401 Q420 Q421 Q419 Q412 Q414 Q407 Q418 Q417



#### **4.9 MCRB ASSY**



SIDE A



SIDE B

# 5. PCB PARTS LIST

NOTES: • Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

- The A mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- When ordering resistors, first convert resistance values into code form as shown in the following examples.

Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

 $0.5 \Omega \rightarrow 5R0$  RN2H[5]ROK  $I \Omega \rightarrow 1R0$ ......RSIP 1 ROK

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).  $5.62k \Omega \rightarrow 562 \times 10^{1} \rightarrow 5621$  RN1/4PC 5 6 2 1 F

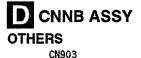
Mark No.	Description	Part No.	Mark No. Description	Part No.
LIST O	F ASSEMBLIES		B PKSB ASSY	
NSP -	EB ASSY LMSB ASSY PKSB ASSY FG ASSY	VWM1507 VWG1554 VWG1555 VWG1556	<b>SWITCHES</b> \$104,\$105	DSG1017
NSP - NSP - NSP -	CHB ASSY CNNB ASSY TNMB ASSY DCSB ASSY LCSB ASSY BISB ASSY	VWM1721 VWG1792 VWG1793 VWG1794 VWG1795 VWG1796	FG ASSY SEMICONDUCTOR D101	GP1S24

Δ	POWER SUPPLY ASSY	VWR1273
NSP NSP	FLKB ASSY (DVL-90/KU/CA) FLKB ASSY (DVL-700/KU/CA) - FLPB ASSY (DVL-90/KU/CA) - FLPB ASSY (DVL-700/KU/CA) - KEYB ASSY	VWM1725 VWM1724 VWG1801 VWG1800 VWG1736

	LEDB ASSY	VWG1832
NSP	CLD MAIN ASSY - CLD MAIN ASSY - JCKB ASSY	VWM1745 VWS1285 VWV1532

DVD MAIN ASSY	VWS1243
FTSB ASSY	VWS1291
MYCB ASSY	VWV1519
MCRB ASSY	VWV1544

D101	GP1S24
MECHB ASSY	
OTHERS	
PC BOARD MECHB	VNP1599



CN903	52030-2310
CN901	52030-2610
CN905, CN906	S2B-PH-K-S
CN902	SLW26R-1C7
CN904	SLW27R-1C7

# TNMB ASSY

CN911

CN912 CN913

MACB ASSY	
OTHERS	
DC DOADD MACD	VMD1.470

<b>HERS</b>			
PC	BOARD	MACB	VNP1479

Ę	DCSB	ASSY
SWI	ТСН	
	S902	

DSG1017

52044-0645 B2B-PH-K-S

B3B-PH-K-S

**LMSB ASSY SWITCHES** 

\$101-\$103 DSG1017

**OTHERS** 

**OTHERS** 

**OTHERS** 10P FFC CONNECTOR CN915

S2B-PH-K-S

CN101

52044-1045

Mark	No.	Descrip	otion	Part No.	<u>Mark</u>	No.	Descrip	tion	Part N	0.
	LCSB #	YSSA			J	FLPB	ASSY			
SWIT				B004417	VWG	1801 and llowing:	VWG1800 h	ave the same	construction e	except for
	S903			DSG1017	416 10	ilowing.		Part	No.	1
OTHE	ERS				Mark	Symbol 8	Description	VWG1801	VWG1800	Remarks
	CN916			S2B-PH-K-S		R111		RD1/4PU202J	RD1/4PU472J	
					• PA	RTS I	IST FOR	R VWG18	01	•
	BISB A	SSY					JCTORS		0.	
SWIT	CH				<u> </u>	IC101			PD4753B	
	S901			DSG1017		IC102 Q102			S-806D DTA124E	e
OTUE	·DC					0101,0	103, Q104		DTC124E	S
OTHE	CN914			S2B-PH-K-S		D101,D	105, D107, D1	80	SLR-342	DUT31
	0,101-1			OZD-I II-K-O		D102,D D104	103, D106		SLR-342 SLR-342	
П	POWER	3 SUPE	PLY ASSY		SWIT	CHES				
	CONDUC					\$101,\$	102		RSG1030	
OLIII.	IC201	010110		AN1431T	CAP	ACITOF	15			
	IC203	2005		UPC358C VZF1047	OAF	C105			CEJA470	M6R3
	1C204, 1C 1C206	203		VZF1047 VZF1048		C103	104 0107 01	00 0111	CKPUYB1	
	0203,020	)4		T7F4S		C102, C	104, C107–C1	09,0111	CKPUYF1	03Z25
	0201,020	)2		T7F4T	RESI	STORS				
<b>A</b>	Q150 Q101			VZF1049 VZF1050		All Re	sistors		RD1/4PU	
Δ	0207,020			2SA933S	отні	EDe				
	0205, 020	06, 0252		2SC1740S	Olli	CN102	FFC BOTTO	M CONNECTOR	5P 52492-0	520
$\Phi$	0102			2SC3377			REMOTE RE	CEIVER UNIT	GP1U28X	
	0251 0213			2SD2007 2SD2395		V101	FL TUBE SPACER		VAW1042 VEC1599	
$\Delta$	D101			D2SB60F4004		CN101	1.25FJ CO	NNECTOR	VKN1375	
$\Phi$	D105			K1V24			FL HOLDER	1	VNF1087	
$\Phi$	D103			MTZJ2.7B		X101	CERAMIC (5		VSS1104	
	D253 D255			MTZJ2.7B MTZJ8.2B						
Δ	D200			PS2501	rr:					
	D207			RD33FB2	K	KEYB	ASSY			
	D206			S2LA20			JCTORS			
Δ	D203 D153			S3L20U VZF1045		0201,0			DTC124E	
43	D230-D23	32		VZF1045		D201, D	202		SLR-342	MCT31
	D202			VZF1051	SWIT	CHES				
	D204, D20	)5		VZF1052	2.111	\$201-S	208		RSG1030	
$\mathbf{\Phi}$	D154 D240			VZF1053 VZF1054						
	D252			VZF1055	CAP	ACITOR			OVBUSE:	02705
Δ	D104			1SS270A		C201, C	202		CKPUYF1	U3ZZ5
	D208, D25			1SS270A	RESI	STORS				
	D209-D21	∠, U254		10ELS2		All Re	sistors		RD1/4PU	
OTHE	RS				ОТН	-RS				
<b>A</b>	F201,F20 F205,F21		FUSE (1A)	VEK1033 VEK1041	<b>51111</b>	CN203	5P FFC C	ONNECTOR	VKN1181	
$\Phi$	F209	•	FUSE (0.5A)	VEK1043		CN201	13P FFC	CONNECTOR	VKN1217	
$\overline{\mathbf{\Phi}}$	F101		FUSE (3. 15A)	VEK1044		CN202	1.25 FJ	CONNECTOR	VKN1375	

<u>Mark</u>	No.	Description	Part No.	Mark	_ <del></del>	Part No.
	LEDB	ASSY			0122, 0181, 0215, 0216, 0652 0901, 0971	DTC124EK DTC124EK
SEMI	CONDI	ICTORS			0910	FMY1A
SCIVII		CIONS	0000014		D221 D311.D505	EC10QS04 KV1851
	Q1-Q3 Q4, Q5		2PD601A UN2212		0311,0303	KA1821
	D1-D3		CL-170SB-X		D181,D650,D655,D821,D881	MA111
	D1-D3		PG1112H-430		D901, D902, D981	MA111
	0.0,		10111211 100		D223, D224	MA152WA
DECK	STORS				D215, D905	MA152WK
REGI		*	PO1 /100 [ [ ]		D851	UDZ2.0B
	All Res	istors	RS1/10S□□□J		D115	UDZ5.1B
OTHE		ELEVIDIE COMMECTOD	10/111 0T A	0011	e AND EILTEDE	
	CN1	FLEXIBLE CONNECTOR	VKN1374	COIL	S AND FILTERS	1 411100 1
					L413 L401	LAU100J LAU101J
					L352, L821-L823	LAU181J
NI	OLD M	AIN ASSY			L251,L252,L311,L331,L351	LAU220J
- ШИ	CLD IV	AIN ASSY			L412, L461, L482, L831, L832	LAU220J
SEMI	CONDU	CTORS			, , ,	
- mm 1011	IC761, I		BA10393F		L411,L587	LAU270J
		C251, IC680, IC903	BA4560F		L431,L432,L575	LAU430J
	IC905, I		BA4560F		L671	LAU4R7J
	1C352		CA0002AM		L462	LAU560J
	IC171, I	C803	LA6510		L414	LAU8R2J
					L463	LFA561J
	1C400		LA7134M LA9420M		F573 14.3MHz FILTER	VTF1055
	1C901 1C801		LA9425		F223	VTF1094
	1C802		LC78681KE		L201, L209, L301, L302, L312	VTL1058
	IC353		M51131L		CHIP COIL(22µH)	
					L207 CHIP COIL(1.5µH)	VTL1059
	1C182, I	C183	MM6558XF		LZO7 CHIP COIL(1.5µh)	41L1039
Δ	1C221		NJM78L08A	CAD	ACITODO	
Δ	1C222 1C208		NJM79L08A NJU6322KE	CAP	ACITORS	
	1C208		PD0236AM		C417, C418, C421, C434, C543	CCSQCH100D50
	10202		DOZJORM		C577, C845	CCSQCH100D50
	10101		PD0246A2		C255, C256, C353, C655, C821 C843, C864, C865, C943	CCSQCH101J50 CCSQCH101J50
	IC201		PD2029AM(L)		C432, C436, C483	CCSQCH120J50
	IC500		PD6159B			000101111111111111111111111111111111111
	IC902		TA8410AK		C412	CCSQCH121J50
	IC181, I	C762, IC907	TC4W53F		C408, C414, C484, C569	CCSQCH150J50
	IC203, I	C201	TC74HC157AF		C355, C823, C901	CCSQCH151J50
	10203, 1 10302, 1		TC74HC4053AF		C313, C352	CCSQCH180J50
	10302, 1	0020	TC7S00F		C205, C509, C824, C973	CCSQCH220J50
	IC102		TC7S32F		C413, C555, C920, C921	CCSQCH221J50
	IC205, I	C209, IC550	TC7SU04F		C550	CCSQCH240J50
			***		C354, C411, C416, C431, C830	CCSQCH270J50
	1C650		TC7W00F		C104, C105, C356, C433, C451	CCSQCH330J50
	1C207 1C204		TC7WH74FU TC7WU04F		C579, C596	CCSQCH330J50
		82, Q482, Q580, Q645	2PB709A		0051 0407 0405 0070	0000011000 150
	0672,09		2PB709A		C351, C407, C485, C672	CCSQCH390J50 CCSQCH391J50
	40,2,40		2. 5. 00.		C671 C222, C257-C260, C405, C461	CCSQCH470J50
	0269,02	70, 0391-0393, 0401	2PD601A		C229, C597	CCSQCH5ROC50
		81, Q625, Q626, Q636	2PD601A		C358, C598, C806	CCSQCH680J50
		47, Q655-Q658	2PD601A			
		62, Q671, Q803, Q811	2PD601A		C435, C822, C829	CCSQCH7ROD50
	usu2-u9	05, Q908, Q909	2PD601A		C357, C825	CCSQCH820J50
	Q834		2SA854S		C459, C462	CCSQCH910J50
	0152		2SC3802K		C230 C656	CCSQCJ3R0C50 CEAL100M16
	0261,02	62	2SD2144S		5555	OENT LOOM LO
		14, 0217, 0394, 0651	DTA124EK		C437	CEAL101M6R3
	Q981		DTA124EK		C927, C931	CEAL220M6R3
					C936, C940	CEAL470M16
					C316	CEAL470M6R3
					C975	CEANP100M16

Mark	No.	Description	Part No.	Mark	No.	De	escription	Part No.
	C263, C264	4, C629, C639	CEANP220M10		C186, C	685. C	355, C926, C938	CKSQYF223Z50
		1, C441, C856	CEANP470M6R3				393, C908, C909	CKSQYF224Z25
		4, C397, C398, C884	CEAS100M50		C154_C	156. C	174, C460, C826	CKSQYF473Z50
	C332, C39		CEASTO1M10		C828, C			CKSQYF473Z50
	C115	•	CEAS102M6R3		, -	,		
	••••		<u> </u>		C923			COMA103J50
	C269, C27	0. C867	CEAS1ROM50		C903			CQMA222J50
		1, C972, C981, C982	CEAS220M25		C265, C	266		CQMA332J50
		2, C934, C977	CEAS2R2M50		C941			COMZA681J50
	C320	_,	CEAS470M10					
		2, C204, C209	CEAS470M16	DECI	STORS	,		
				RESI		•		
	C223, C22	4, C261, C262, C302	CEAS470M16		R753			RA4C221J
	C304, C31	7, C382, C390, C396	CEAS470M16		R203, R			RA4C471J
i	C802, C804	4, C832, C834, C842	CEAS470M16				834, R837, R839	RN1/10SE1002D
	C852, C85	4, C859, C860	CEAS470M16		R891,R			RN1/10SE1002D
	C253, C25		CEAS471M10		R152, R	156		RN1/10SE1003D
					0500			DN1 /10051100D
	C862, C98	4	CEAS4R7M50		R532			RN1/10SE1100D
	C383, C91	6, C922	CEASR47M50		R531	000 D	20.4	RN1/10SE1800D
	C439		CEV100M16		R151,R			RN1/10SE3302D
		3, C475, C507, C531	CEV101M6R3			134, 62	259-R262	RN1/10SE4702D
	C535, C53	7, C539, C541, C561	CEV101M6R3		VR450		(2.2kΩ)	PCP1025
					VR603		(4.71.0)	DCD1000
	C571,C58	1, C591, C593	CEV101M6R3			VDene	(4.7kΩ)	PCP1028
	C928		CFTXA104J50				, VR607, VR609 (47kΩ)	PCP1031
	C477, C91	1,C929	CFTXA154J50		Other	Kesis	tors	RS1/10S□□□J
	C930		CFTXA473J50					
	C478		CFTXA683J50	OTHE	ERS			
					CN312		6P FFC CONNECTOR	52045-0645
		0, C917, C918	CKSQYB102K50		CN103,	CN311	10P FFC CONNECTOR	52045-1045
	C942		CKSQYB104K25		CN301		15P FFC CONNECTOR	52045-1545
	C925		CKSQYB332K50		CN802		11P TOP POST	B11P-SHF-1AA
	C379, C38		CKSQYB392K50		CN215		KR CONNECTOR	B2B-PH-K-E
	C371-C37	6, C388, C912	CKSQYB472K50					
	0700		OKOOMDOOKEO		CN104,	CN208	KR CONNECTOR	B2B-PH-K-S
	C763		CKSQYB682K50		CN803		3P TOP POST	B3P-SHF-1AA
		2, C121, C124, C153	CKSQYF103Z50		CN101		B TO B CONNECTOR 12P	BTFN12S-3SB7
		3, C181, C183, C184	CKSQYF103Z50		CN102		B TO B CONNECTOR 12P	BTFN20S-3SB7
	C188, C18	9, C201, C203	CKSQYF103Z50		JA331		OPTICAL MODULE	GP1F32T
	C206-C20	8, C210, C213, C214	CKSQYF103Z50					
	COST COE	1, C252, C281-C283	CKSQYF103Z50				PCB BINDER	VEF1040
		3, C311, C312, C315	CKSQYF103Z50		JA252		4P PIN JACK	VKB1070
		9, C331, C361, C362	CKSQYF103Z50		JA251	-	1P PIN JACK	VKB1074
		6, C389, C395, C422	CKSQYF103Z50				64P IC SOCKET	VKH1004
		0, C511, C558	CKSQYF103Z50		CN502		26P FFC CONNECTOR	VKN1202
	0442,001	0,0311,0330	OKO411 100200		011001		070 550 000050700	WHIOO
	C575, C576	6, C580, C583, C587	CKSQYF103Z50		CN801		27P FFC CONNECTOR	VKN1203 VKN1206
		2, C801, C803, C811	CKSQYF103Z50		CN121		30P FFC CONNECTOR	
		1, C833, C841, C846	CKSQYF103Z50		X101	CEDAN	SCREW TERMINAL IC RESONATOR (9.00MHz)	VNE1948
	C851, C85	3, C861, C881-C883	CKSQYF103Z50				AL RESONATOR (16MHz)	VSS1040 VSS1081
	C885. C92	4, C935, C937, C939	CKSQYF103Z50		VOLL	UNISIA	AL RESUNATOR (TOMB2)	4221001
	,		-		¥212	CHIP	CRYSTAL (36.86MHz)	VSS1085
	C945, C94	6, C961, C962, C974	CKSQYF103Z50				AL RESONATOR(14MHz)	VSS1083 VSS1103
	C983	,	CKSQYF103Z50		VOO	Chion	SCREW	BBZ30P060FCC
	C101, C10	3, C122, C151, C152	CKSQYF104Z25				SCHEN	DD2301 0001 00
	C171, C17	2, C182, C227, C228	CKSQYF104Z25					
	C267, C26	8, C385, C387, C392	CKSQYF104Z25					
				M	101/5	404	<b>0</b> 1/	
	C402, C40	4, C419, C430, C438	CKSQYF104Z25	LV.	<b>JCKB</b>	AS:	<b>3</b> 1	
		5, C447, C472, C474	CKSQYF104Z25	CEAN	יטואט	ICT	)De	
		8, C524, C532, C536	CKSQYF104Z25	2FIAI	COND			
	C538, C54	0, C542, C556, C557	CKSQYF104Z25		IC321,	1C322		TC74HCU04AF
	C562, C57	2, C582, C586, C589	CKSQYF104Z25		D341			MA111
		4, C620, C622	CKSQYF104Z25	COIL	S			
		8, C630, C636, C638	CKSQYF104Z25		L322,L	326		LAU1R0J
		1-C683, C764, C805	CKSQYF104Z25		L322, L			LAU220J
		8, C866, C886	CKSQYF104Z25		L323,L		PAL TRANS.	PTL1003
	C913-C91	5, C919, C963, C976	CKSQYF104Z25		LJZJ, L		IAL IIIANO.	. 121000

Mark	No. Description	Part No.	Mark	No.	Description	Part No.
					, 0741, 0792, 0814	2PB709A
CAPA	CITORS			Q848, Q857		2PB709A
	C322, C324, C326, C328	CEAL470M16				
	C323, C327, C341-C345	CKSQYF103Z50			, 0471, 0472	2PD601A
	C3460, C3480	CKSQYF104Z25			, 0605, 0669, 0701	2PD601A
	C3400, C3480	CR3011 104223		0742,0771	, 0773, 0793, 0845, 0851	2PD601A
DECK	TODE			0014 0016	0005 0006 0046	ODDCO1 A
HEOK	STORS				, Q925, Q936, Q946	2PD601A
	All Resistors	RS1/10S□□□J		0381		2SB1260
				0712-0715		2SC3802K
OTI IT	'DC			Q103		DTA114EK
OTHE	:H5			Q104, Q617.	, 0618, 0772, 0811	DTC114EK
	JA321, JA322 REMOTE CONTROL JACK	RKN1004				
	JA324 1P PIN JACK	VKB1074		0101,0102	. 0105	DTC114TK
	JA323 1P PIN JACK	VKB1097		0886, 0887		DTC124EK
	SCREW TERMINAL	VNE1948		D786, D787		188355
		1112.010			, D981, D982	DAN202K
				D110	, 5501, 5502	EC10QS04
				5110		20104004
	OVE BAAIN ACCV			D761		KV1410
	OVD MAIN ASSY			D101		RB501V-40
CEMI	CONDUCTORS			D640		UDZ2.0B
SEIMI		2110002				
	IC631, IC981	BA10393F	COIL	S AND FIL	TERS	
	IC851	BA6797FP				
	IC901	CXA2521AQ		L321	CHIP SOLID INDUCTOR	ATL7001
	1C801	CXD2545Q				DTL1028
	IC101	HD6417032F20		F541	DVD VIDEO FILTER	VTF1072
				F535, F536,	F538, F539 FERRITE BEAD	VTF1073
	1C162	HM514800CJ-7		F537	FERRITE BEAD	VTF1074
	1C995	IR3C07N				
	IC531, IC535	MB81C4256A-70PJ		F1491	FERRITE BEAD	VTF1075
	IC551	MC14577CF			FERRITE BEAD	VTF1076
	IC231, IC621, IC781, IC931	NJM2100M		F199		VTF1077
	10231, 10021, 10701, 10931	NOME TOOM		F704		VTF1078
	10071 10070 10700 10701 10071	N 84000 444				
	IC671, IC672, IC732, IC791, IC971	NJM2904M		F390-F399	FERRITE BEAD	VTF1079
	IC831, IC911	NJM4580M				
	IC601	PA0065AM			-F188 FERRITE BEAD	VTF1080
	IC161	PD4695A		L431, L432,		VTL1058
	IC501	PD4696A			CHIP COIL(22µH)	
				L701, L761,	L801 CHIP COIL(22µH)	VTL1058
	IC201	PD4784A		L762	CHIP COIL(1.5µH)	VTL1059
	IC165	PD4795A			•	
	IC104	PDK022A		L501.L592	CHIP COIL (0.15µH)	VTL1060
Δ	IC381	TA78M08F				VTL1061
212	IC471, IC815, IC820	TC4W53F		L401	CHIP COIL (22µH)	VTL1062
	10471, 10013, 10025	10411031		L421	CHIP COIL (47µH)	VTL1063
	IC102	TC558128AJ-20		L-72 I	OIII 0012(47 p.11)	112,000
	IC204	TC74HC20AF				
			CAPA	CITORS		
	1C972	TC74HC4052AF		C509		CCSRCH100D50
	IC921	TC74HC4053AF		C800		CCSRCH101J50
	1C832	TC74HC4066AF		C601-C604,	CENE CON	CCSRCH121J50
				C902, C903	, 0000, 0904	CCSRCH151J50
	IC202	TC74HC573AF				
	IC641, IC761	TC74HCU04AF		C723		CCSRCH180J50
	IC302	TC7S04F		2000		0000011101 150
	IC105	TC7SH02F		C620		CCSRCH181J50
	IC106	TC7SH32F		C716, C810,	, C917	CCSRCH221J50
				C508, C618		CCSRCH270J50
	IC311	TC7ST08F		C765		CCSRCH330J50
	IC751	TLC272CPS		C914		CCSRCH390J50
	IC731	TLC5540 INS				
				C862-C864		CCSRCH391J50
	10421	UPD4516161G5-A12-7JF		C730, C814		CCSRCH470J50
	IC401	UPD61021		C616, C681		CCSRCH471J50
				C724		CCSRCH560J50
	1C1030	VYW1515			6714	
	1C2050	VYW1516		C556, C566,	C/14	CCSRCH5R0C50
	IC301	ZR38521				
	Q473, Q481-Q485, Q551, Q552	2PB709A		C634, C806,	C854, C855	CCSRCH680J50
	Q561, Q562, Q591, Q667, Q702	2PB709A		C107, C108		CCSRCH7R0C50
	2211 20021 20011 2001 , 2102			C813		CCSRCH820J50
				C476		CCSRCH910J50
					C159, C162, C180	CEV101M6R3
				-,		

Mark	No. Description	Part No.	Mark	No. Description	Part No.
	C401, C420, C430-C440	CEV101M6R3		C738, C739, C750, C761, C781	CKSRYF104Z16
	C500, C501, C523, C532, C533	CEV101M6R3		C799, C802, C803, C805, C812	CKSRYF104Z16
	C536-C540, C801, C821	CEV101M6R3		C818, C820, C822, C823, C829	CKSRYF104Z16
	C755	CEV1ROM50		C831, C858, C901, C911, C918	CKSRYF104Z16
	C325, C384, C571, C592, C857	CEV220M16		C921, C930, C971, C972	CKSRYF104Z16
				C980-C982, C995	CKSRYF104Z16
	C859	CEV220M16			
	C611, C712, C731, C733, C900	CEV220M6R3		VC510, VC765 (20pF)	VCM1008
	C912, C919, C994	CEV220M6R3			
	C179, C201, C321, C327, C396	CEV470M6R3	RESIG	STORS	
	C493, C517, C591, C701, C804	CEV470M6R3	ILLON		
					RA4C103J
	C996	CEV470M6R3			RA4C103J
	C720, C787	CEVNP100M16			RA4C220J
	C789	CEVNP2R2M35			RA4C220J
	C908	CFH\$333J16		R251-R257, R266, R274	RA4C220J
	C788, C839, C840	CFHS473J16		5404 5400 5404 5405 5404	D. 10000 !
					RA4C220J
	C884, C885, C907	CFHSP104J16			RA4C220J
	C686, C909	CFHSQ103J16			RA4C220J
	C882, C883	CFHSQ272J50			RA4C390J
	C677	CFHSQ822J16		R723, R2510, R2620, R2630	RS1/10S0R0J
	C843, C844, C894	CKSQYB104K25			
					RS1/10S0R0J
	C615, C680, C713, C718, C742	CKSQYB105K10			RS1/10S1R2J
	C746, C747, C751, C811	CKSQYB105K10			RS1/16S1001F
	C815, C817	CKSQYB224K16			RS1/16S1002F
	C759, C893	CKSQYB474K16		R149, R166, R477, R693	RS1/16S1003F
	C206, C207, C441-C446, C519	CKSQYF225Z16			
					RS1/16S1003F
	C527-C530	CKSQYF225Z16			RS1/16S1003F
	C749, C766	CKSRYB102K50			RS1/16S1202F
	C101, C121, C169, C178	CKSRYB103K50			RS1/16S1502F
	C471, C472, C574, C605, C617	CKSRYB103K50		R580, R582, R783, R784	RS1/16S2202F
	C676, C700, C711, C762, C764	CKSRYB103K50			
	, , , ,			R835-R840, R871, R872, R893	RS1/16S2202F
	C816, C830, C832, C837, C838	CKSRYB103K50			RS1/16S2202F
	C853, C861, C881, C906	CKSRYB103K50			RS1/16S2203F
	C997-C999	CKSRYB103K50			RS1/16S2203F
	C983, C984	CKSRYB104K16		R712, R720, R857	RS1/16S3901F
	C809	CKSRYB152K50			
					RS1/16S4702F
	C692	CKSRYB153K50			RS1/16S4702F
	C641-C644, C649, C819	CKSRYB222K50			RS1/16S4702F
	C931, C932	CKSRYB222K50			RS1/16S4703F
	C847	CKSRYB332K50		R575, R741, R742	RS1/16S5601F
	C741	CKSRYB472K50			/
					RS1/16S5602F
	C735, C808	CKSRYB473K16			RS1/16S6802F
	C102-C106, C109-C111	CKSRYF104Z16			RS1/16S8202F
	C113-C115, C120, C155-C158	CKSRYF104Z16		* · · · · · · · · · · · · · · · · · · ·	VCP1090
	C160, C161, C163-C167	CKSRYF104Z16		VR904, VR921 (10KΩ)	VCP1092
	C170, C171, C173-C177, C181	CKSRYF104Z16		VB001 1/B000 (00"0)	V0D1004
					VCP1094
	C184-C187, C191, C192	CKSRYF104Z16		· · · · · · · · · · · · · · · · · · ·	VCP1131
	C202-C205, C209, C231	CKSRYF104Z16		Other Resistors	RS1/16S∐∐∐J
	C300-C303, C305-C307, C309	CKSRYF104Z16			
	C311, C322, C326, C328	CKSRYF104Z16	OTHE	RS	
	C382, C383, C391-C393, C395	CKSRYF104Z16			S2B-PH-SM3
				32P IC SOCKET	VKH1011
	C397, C399, C402-C417	CKSRYF104Z16			VKH1012
	C421-C426, C473-C475, C481	CKSRYF104Z16		CN601, CN602 B TO B CONNECTOR 60P	
	C483, C484, C491, C492	CKSRYF104Z16		•	VKN1299
	C502-C507, C510-C516, C518	CKSRYF104Z16		OHIOS / ITO COMMECTOR	11011244
	C520-C522, C526, C531, C535	CKSRYF104Z16		CN101 13P FFC CONNECTOR	VKN1305
					VKN1316
	C553-C555, C563, C565	CKSRYF104Z16		CN902 B TO B CONNECTOR 14P	
	C572, C573, C577, C596, C607	CKSRYF104Z16			VKN1324 VKN1345
	C612, C613, C621, C630, C631	CKSRYF104Z16		26P FFC CONNECTOR	11011010
	C640, C671, C675, C683	CKSRYF104Z16		ZOI ITO COMMECTOR	
	C702-C704, C721, C732, C734	CKSRYF104Z16			

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	CN251	30P FFC CONNECTOR	VKN1349	COILS			
	VEA1	INSPECTION LABEL	VRW1634 VSS1086		L401-L	403	LAU220J
	X501 X201	CHIP CRYSTAL(27.00MHz) CHIP CERAMIC(5.00MHz)	VSS1000 VSS1102				
	X301	CHIP CERAMIC(33.000MHz)	VSS1105	CAPA	ACITOF	RS	
		,		<b></b>	C433	••	CCSQCH100D50
	X101	CHIP CERAMIC(20.00MHz)	VSS1106		C401, C	404	CCSQCH220J50
					C405		CCSQCH470J50
					C403		CCSQCH560J50
					C402		CCSQCH6R0D50
124	FTSB	ASSY			C411		CCCCCU010 IEO
CEM	COND	UCTORS				103, C109, C111, C113	CCSQCH910J50 CEAS101M10
SEIVI			D410000F			212, C214, C216, C301	CEASIOIMIO
	1C204, 1C301	1C306, 1C403	BA10393F MC14577CF			309, C311, C317, C319	CEAS101M10
		IC303, IC305, IC401	NJM072BM			424, C426, C429, C431	CEAS101M10
	10302,	10000, 10000, 10401	NJM2100M				
	IC304,	IC402	NJM4580M			436, C438	CEAS101M10
					C303	104 (110 (110 (114	CKSQYB102K50
		309, 0401-0403	2PB709A			104, C110, C112, C114 118, C213, C215, C217	CKSQYF104Z25 CKSQYF104Z25
		1303, Q305, Q404	2PD601A			304, C306-C308, C310	CKSQYF104Z25
	0304,0	1308 1206, D303, D305-D307	DTC114EK 1SS355		,-	. ,,	
		0401, D402	1SS355			316, C318, C320-C322	CKSQYF104Z25
	20.0,0		10000			407, C413, C414, C423	CKSQYF104Z25
	D308		DAN202K			427, C428, C430, C432	CKSQYF104Z25
					6435,6	437, C439, C442, C447	CKSQYF104Z25
CAP	CITO	<b>3</b> 5		DECI	STORS		
	C316		CCSRCH101J50	RESI		•	DU1 /100F1001D
	C401, C	501	CEV100M16		R424 R422		RN1/10SE1801D RN1/10SE2201D
	C303	1400	CFHS473J16		R309		RN1/103E2201D
	C306, C		CFHSQ471J50 CKSQYB105K10		R425		RN1/10SE2702D
	C209, C	210, C305	CKSQIDIOSKIO		R310, R	420, R421	RN1/10SE3301D
	C308, C	C403, C406	CKSRYB102K50				
	C311	.,,	CKSRYB472K50		R312, R	426	RN1/10SE4701D
	C313		CKSRYB473K16		R311 VR301	(22kΩ)	RN1/10SE5601D PCP1030
	•	211, C302, C304, C307	CKSRYF104Z16			(22KS2) Resistors	RS1/10S□□□J
	C309, C	312, C314, C315, C402	CKSRYF104Z16		Other	1103131013	101710000000
	C404, C	:407	CKSRYF104Z16	OTHE	ERS		
	C310	,,,,,,	CCSRCH101J50	<b>U</b> 1111	CN104	10P FFC CONNECTOR	52045-1045
	C405		CKSQYB224K16		CHIOT	2P PIN JACK	AKB7076
					CN101	B TO B CONNECTOR 12P	BTFN12P-3RD7
RESI	STORS	8			CN102	B TO B CONNECTOR 20P	BTFN20P-3RD7
	R322		RS1/16S1001F			4P MINI DIN SOCKET	VKN1078
	R405		RS1/16S1801F			OCOUNT TEDMINA	VAIC1040
	R406		RS1/16S4701F			SCREW TERMINAL SHIELD CASE A	VNE1948 VNF1098
	R321		RS1/16S5601F			SHIELD CASE C	VNF1100
	0ther	Resistors	RS1/16S□□□J			OHIELD VIVE V	*,4 1100

### **OTHERS**

CN101, CN102 B TO B CONNECTOR 30P VKN1294

# MYCB ASSY SEMICONDUCTORS

IC301	CXD2046Q
IC102, IC103	MB81C1501PF
IC101	PD3212A
Q402, Q404, Q407, Q411, Q414	2PB709A
0401,0403,0412,0413	2PD601A
Q408-Q410, Q415, Q416	2SC1740S
0417,0420	DTA124EK
0418,0419,0421	DTC124EK

Mark No. Description	Part No.	Mark No. Description	Part No.
R MCRB ASSY		R73 R75	RS1/10S47R0F RS1/10S5600F
SEMICONDUCTORS		R81	RS1/10S68R0F
1016, 1017	NJM2100M	Other Resistors	RS1/10S□□□J
IC101	PD9014A	OTHERS	
IC51	TC4W53F	X11 CRYSTAL(3.579545MHz)	VSS1107
C15,  C52  C11	TC74HC4053AF TC74HCU04AF	PCB BINDER	VEF1040
	10/4/1000474	CN12 26P FFC CONNECTOR	VKN1202
IC171	TC74VHCT374F	EARTH METAL FITTING	VNF1084
IC18 Q252, Q59	TC7WU04F 2PB709A		
Q11	2PD601A		
Q13	DTC124EK		
Q55, Q56, Q60	IMT1A		
0254, 051	IMX1		
Q12, Q253, Q52-Q54 Q57, Q58	1MZ1A 1MZ1A		
D11	SVC201SPA		
0011.0			
COILS	1 41070 1		
L271 L272	LAU270J LAU390J		
L273	LAU430J		
L11	LFA220J		
CAPACITORS			
C274, C30	CCSQCH100D50		
C22	CCSQCH180J50		
C15 C275,C277	CCSQCH221J50 CCSQCH330J50		
C276	CCSQCH390J50		
C171, C173, C174, C179	CCSQCH470J50		
C24	CCSQCH910J50		
C16, C19 C1, C110, C122, C126, C152	CEJA101M10 CEJA470M10		
C2, C208, C301, C305, C306	CEJA470M10		
C313, C4, C52, C53, C55	CEJA470M10		
C62, C64	CEJA470M10		
C12	CFTXA104J50		
C13 C11, C18, C20, C25, C26	CFTXA334J50 CKSQYF103Z50		
C500 C107, C109, C113, C115, C121	CKSQYF103Z50 CKSQYF104Z25		
C125, C153, C17, C207, C215	CKSQYF104Z25		
C217, C219, C220, C255, C28	CKSQYF104Z25		
C302-C304, C307-C312, C314	CKSQYF104Z25		
C51, C54, C56-C61, C65	CKSQYF104Z25		
C67 C14	CKSQYF104Z25 CQMZA682J50		
VC11 (20pF)	VCM-008		
RESISTORS	DU1 /100F1001D		
R52 R51	RN1/10SE1801D RS1/10S1000F		
R74	RS1/10S1001F		
R77 R71	RS1/10S10R0F RS1/10S1501F		
	·		
R72	RS1/10S1802F		
R76 R79	RS1/10S27R0F RS1/10S3300F		
R80	RS1/10S3900F		
R78	RS1/10S39R0F		

### 6. ADJUSTMENT (調整方法)

#### 6.1 ADJUSTMENT ITEMS AND LOCATION (調整項目と調整位置)

#### Adjustment Items

[Mechanical Part]

#### CLD

- Tilt Offset Adjustment (チルトオフセット調整)
- Tangential Direction Angle Adjustment for Side A (A面タンジェンシャル傾き調整)
- Spindle Motor Centering Adjustment for Side A (A面スピンドル芯出し調整)
- Crosstalk Check and Fine Tilt Offset Adjustment for Side A (A面クロストーク確認及び、チルトオフセット微調整)
- Focus Servo Loop Gain Adjustment (フォーカスサーボループゲイン調整)
- 6 Tracking Servo Loop Gain Adjustment (トラッキングサーボループゲイン調整)
- Tangential Direction Angle Adjustment for Side B (B面タンジェンシャル傾き調整)
- Spindle Motor Centering Adjustment for Side B (B面スピンドル芯出し調整)
- Crosstalk Check and Fine Tilt Offset Adjustment for Side B (B面クロストーク確認及び、チルトオフセット微調整)

#### DVD

- 10 DVD Focus S-curve Level Coarse Adjustment (DVDフォーカスS字レベル粗調整 )
- **1** RF MAX Adjustment (RF MAX調整)
- ① Jitter Adjustment (ジッター調整)
- Tracking Error Level Adjustment (トラッキングエラーレベル調整)
- OVD Focus S-curve Level Fine Adjustment (DVDフォーカスS字レベル微調整)

### [Electricall Part]

### CLD

- ① Video Level Adjustment (ビデオレベル調整)
- ② PLL Offset Adjustment (PLLオフセット調整)
- ③ Y Output Level Adjustment (Y出カレベル調整)

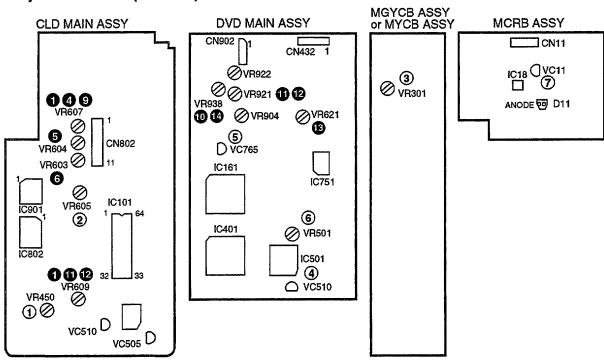
### DVD

- Master Clock Adjustment (マスタークロック調整)
- (5) VCO Offset Adjustment (VCOオフセット調整)
- ⑥ Video Output Adjustment (ビデオ出力調整)

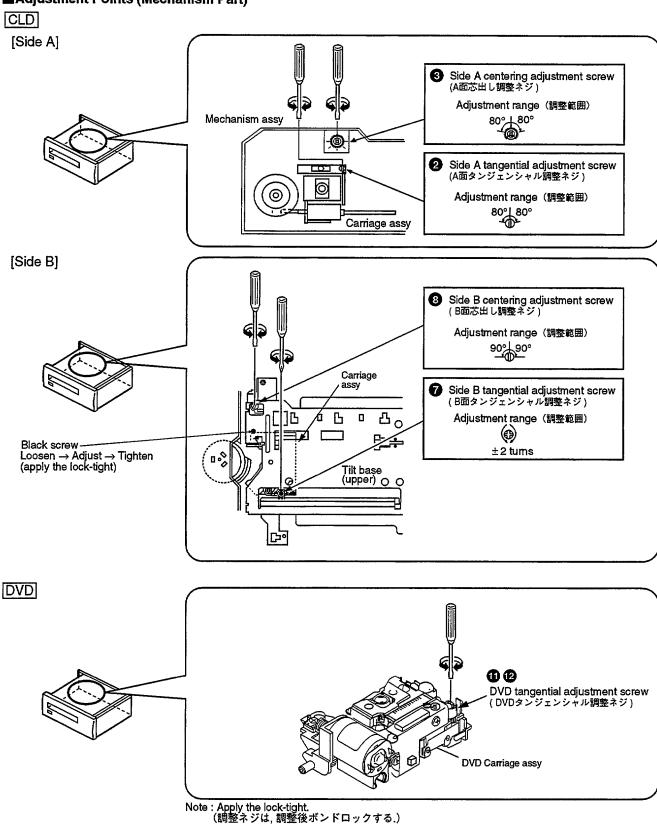
### MCRB

⑦ MCRB Master CLK Adjustment (MCRBマスターCLK調整)

### Adjustment Points (PCB Part)



### ■Adjustment Points (Mechanism Part)

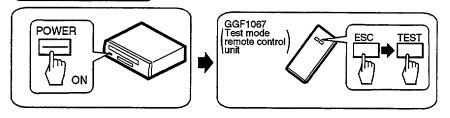


### 6.2 JIGS AND MEASURING INSTRUMENTS (調整に必要な治工具類)

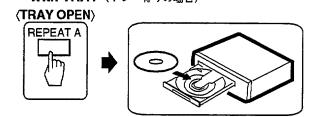
CD test disc (YEDS-7)	LD test disc (GGV1012)	DVD test disc (DVD-MJK1)	⊝ Screwdriver (medium)
⊝ Screwdriver (small)	+ Precise screwdriver	<ul><li>☐ Precise screwdriver</li></ul>	① Screwdriver (large)
① Screwdriver (medium)		CH1 CH2  (X) (Y)  CH1 CH2  (X) (Y)  CH1 CH2  (X) (Y)  CH1 CH2  (X) (Y)  (X)  (Y)  (X)  (Y)  (Y)  (Y)  (Y)	○ 8888888 Frequency counter Display digit ≧ 8-digit
TV monitor	Test mode remote control unit (GGF1067)	Jitter meter	O O  Equalizer unit

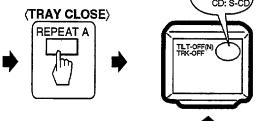
### **6.3 TEST MODE** (テスドモード)

### **TEST MODE: ON**



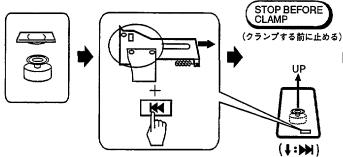
# TEST MODE: DISC SET • With TRAY (トレー有りの場合)

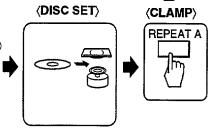




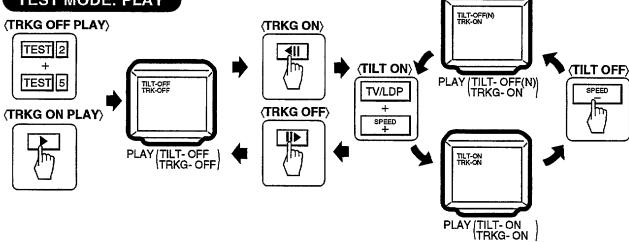
CHECK DVD, LD: S-LD

### ◆ No TRAY (トレー無しの場合)

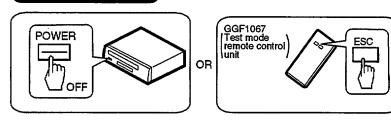




### TEST MODE: PLAY



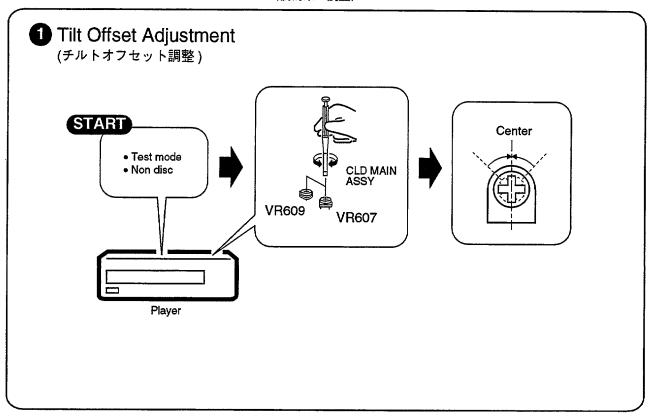
### **TEST MODE: OFF**

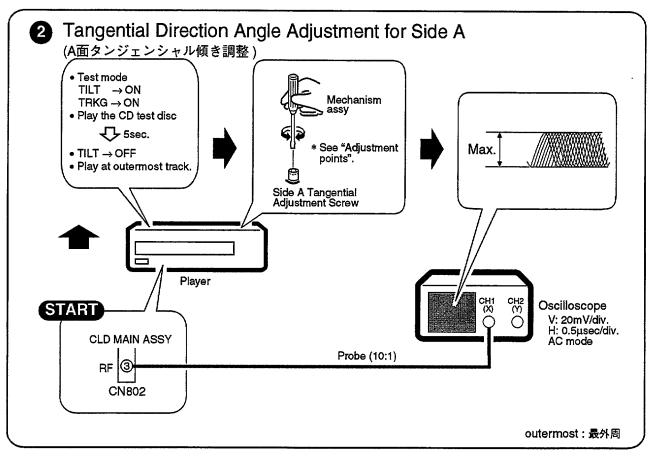


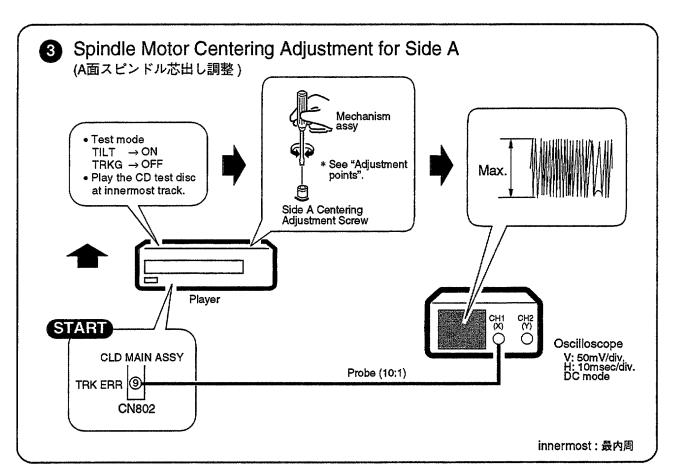
### **6.4 NECESSARY ADJUSTMENT POINTS**(必要な調整項目)

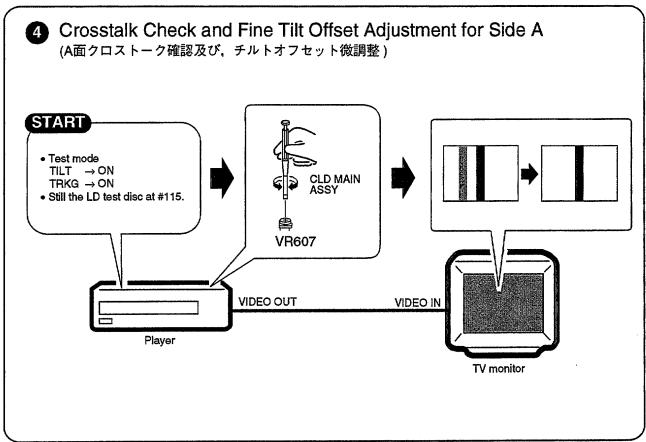
When (このような時) ■ EXCHANGE MECHANISM ASSY PARTS (メカASSY部品を交換したとき)	Adjustment Points
Exchange pickup (CLD) (CLDのピックアップを交換したとき)	Mechanical point 1,2,3,4,5,6,7,8,9  Electric point
Exchange pickup (DVD) (DVDのピックアップを交換したとき)	Mechanical point 0,0,12,13,14  Electric
Exchange spindle motor (スピンドルモータを交換したとき)	Mechanical 9,8  Electric
■ EXCHANGE PCB ASSY (PCB ASSYを交換したとき)	point
Exchange board CLD MAIN ASSY (マザーボードを交換したとき)	Mechanical 1,4,5,6,9  Electric point
Exchange board DVD MAIN ASSY (マザーボードを交換したとき)	Note:①,② and③ are adjusted already.(①,②,③は調整済)  Mechanical
Exchange board MCRB ASSY	point Note: ④, ⑤ and ⑥ are adjusted already. (④,⑤,⑥は調整済)  Mechanical point
(MCRB ASSYを交換したとき)	Electric point Note: ⑦ is adjusted already. (⑦は調整済)

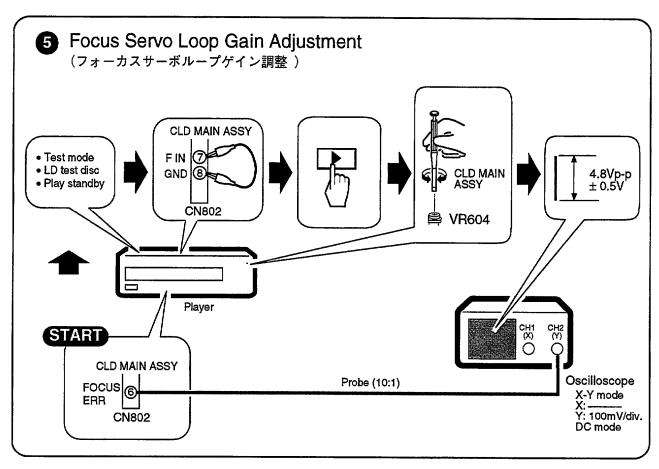
### 6.5. MECHANICAL ADJUSTMENT (機構系の調整)

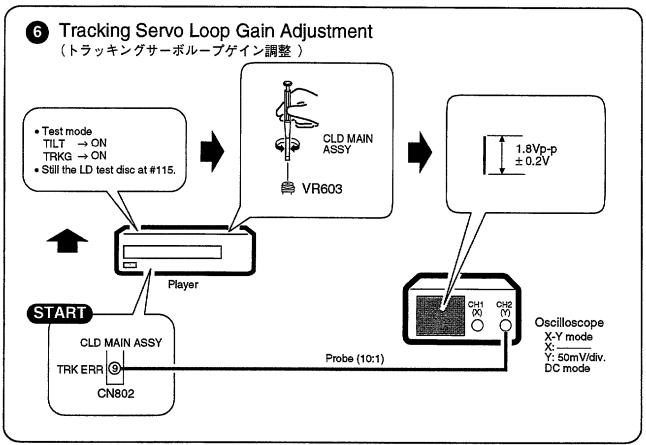


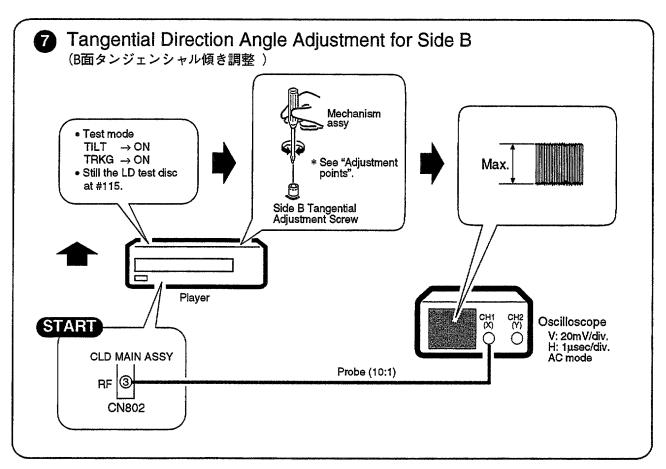


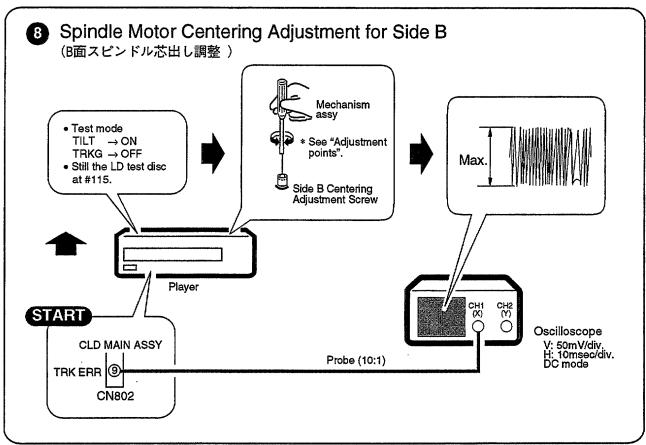


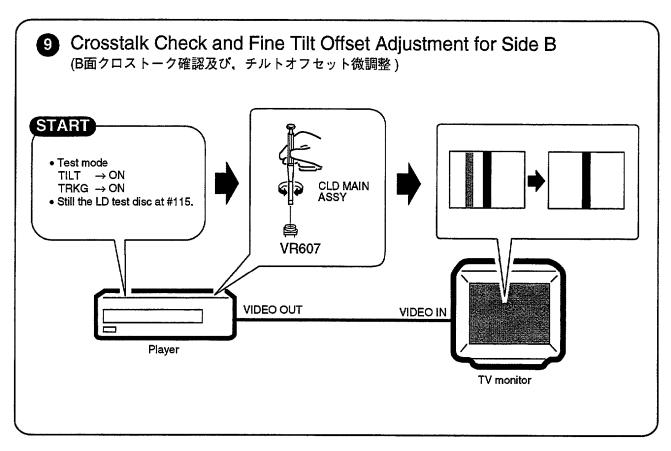


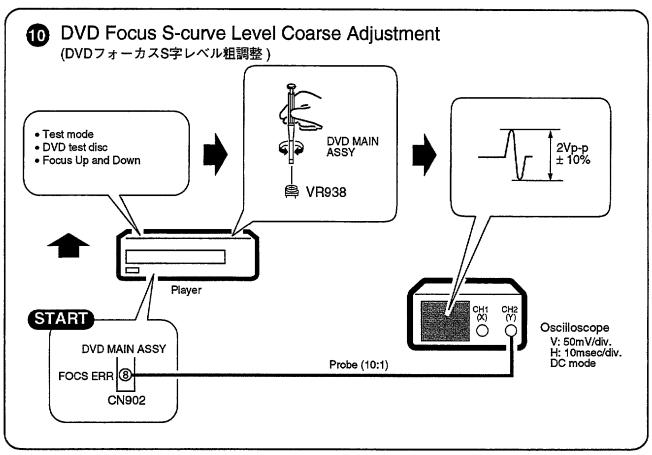


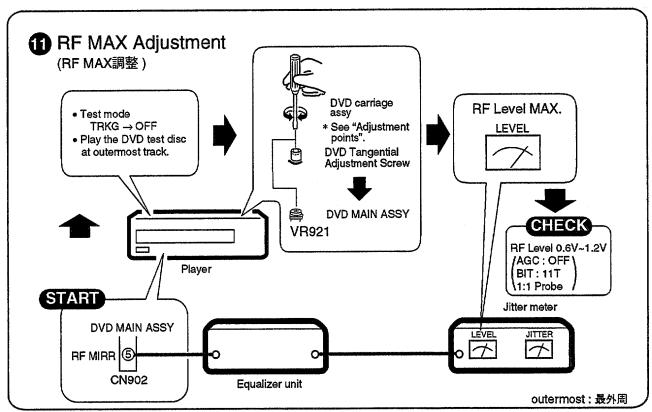


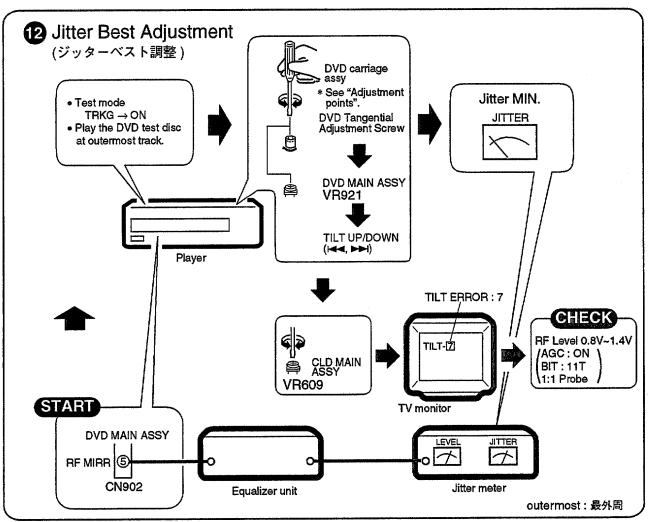


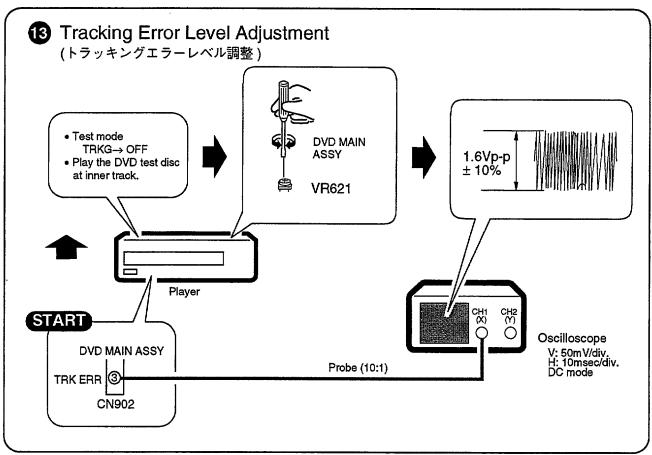


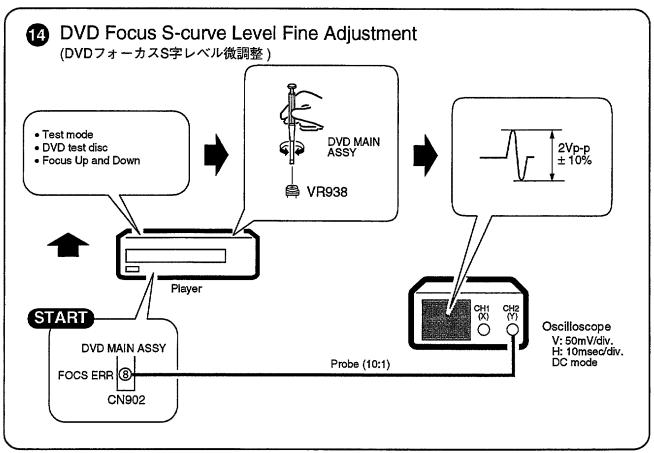




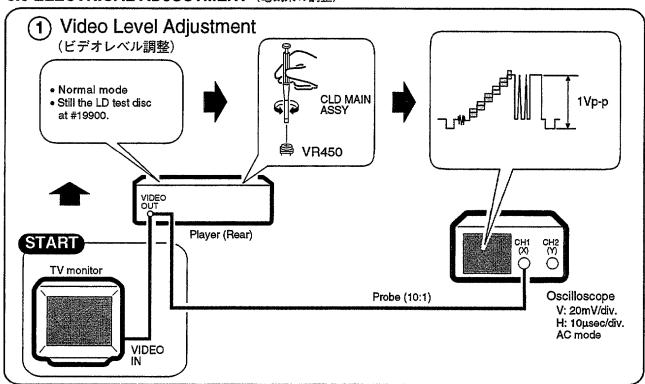


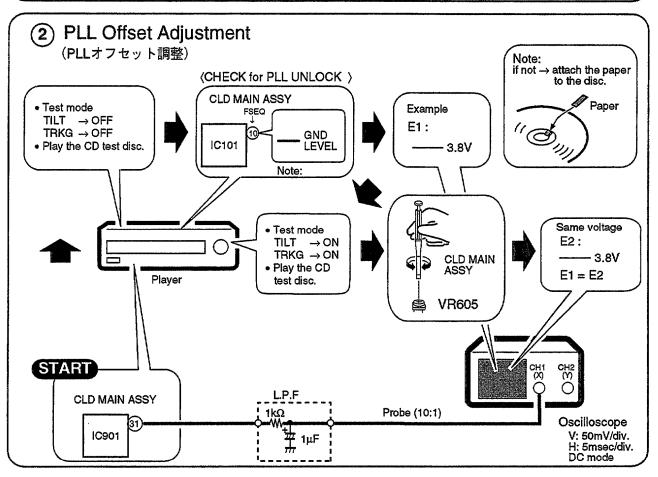


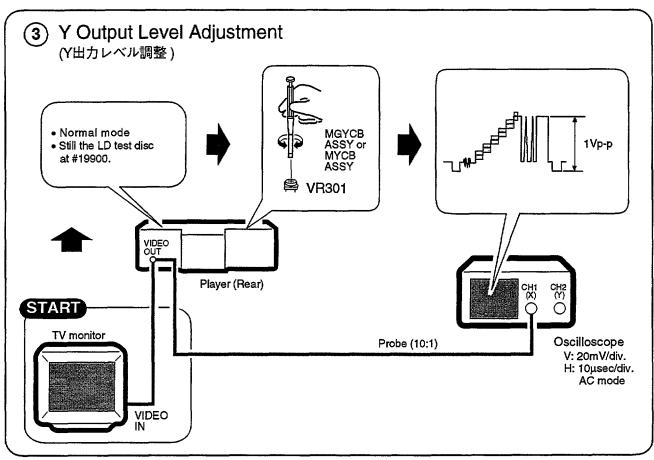


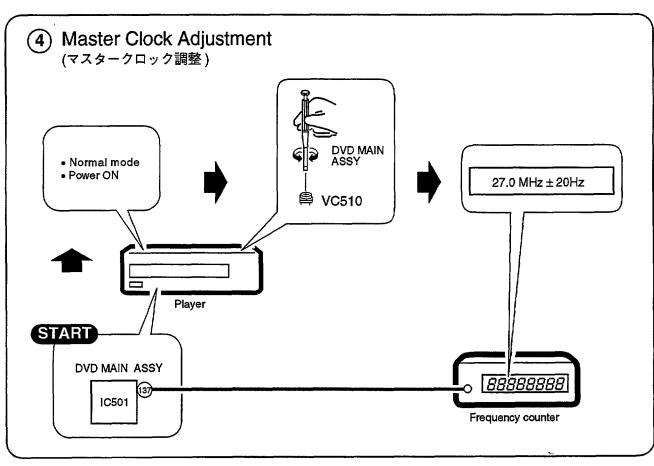


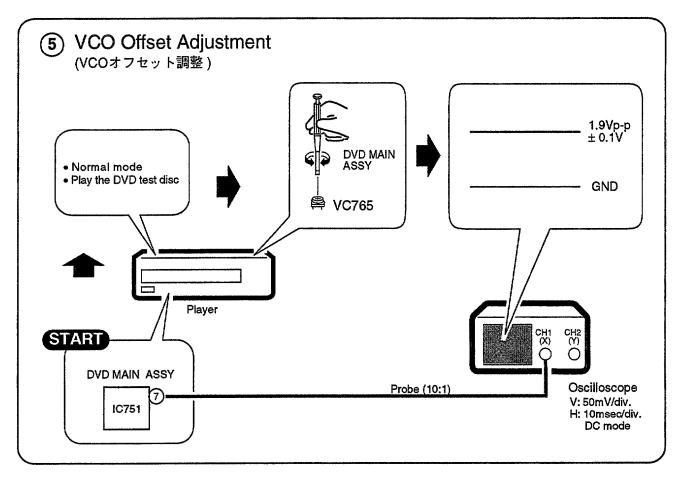
### 6.6 ELECTRICAL ADJUSTMENT (電気系の調整)

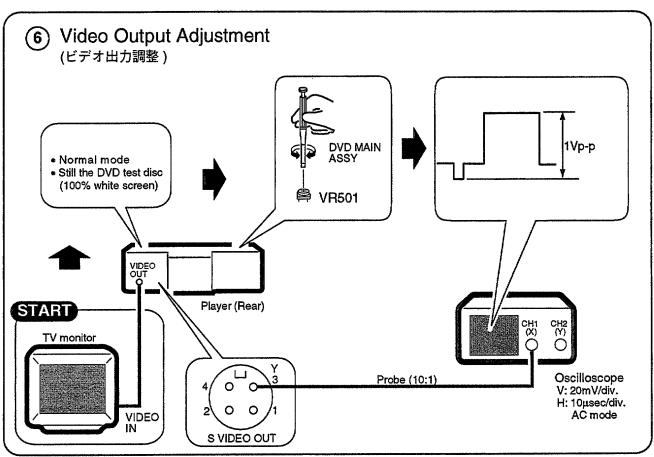


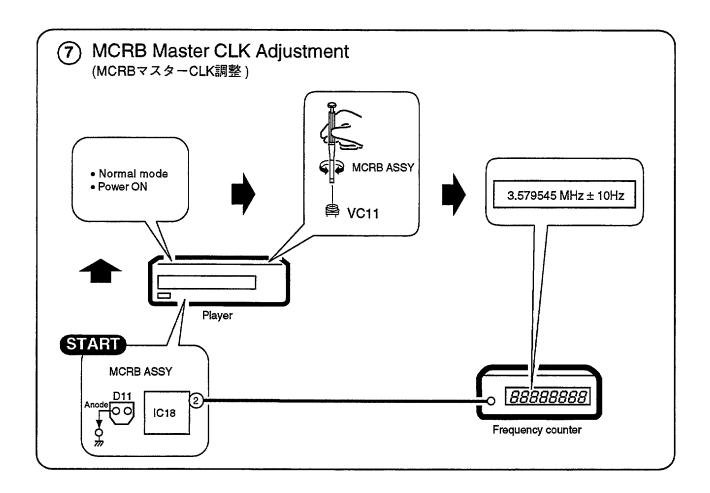






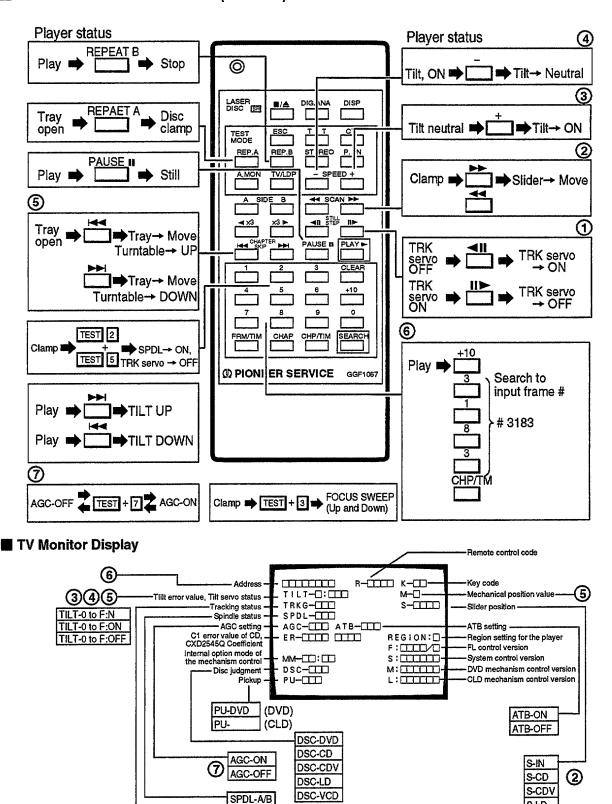






### 6.7 OPERATIONS IN THE TEST MODE (テストモード時のサービス用リモコン操作方法)

#### **■** Test Mode Remote Control Unit (GGF1067)



SPDL-FG

SPDL-SRV

SPDL-O-S

TRK-ON

(1) TRK-OFF

S-LD

S-B IN

# 7. GENERAL INFORMATION

### **7.1 PARTS**

### 7.1.1 IC

• The information in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

# ■ PD4753B (FLPB ASSY : IC101)

• MODE CONTROL IC

No.	Name	Function Name	ΙO	Function	ACTIVE
1	P94	T6	0		
2	P93	T5	0		
3	P92	T4	0		
4	P91	T3	0	FL timing output.	H:ON
5	P90	T2	0		
6	P81	T1	0		
7	P80	TO	0		
8	VDD	Vcc	1-	-	-
9	P27	Angle LED	0	Angle LED ON/OFF.	H:ON
10	P26	SIDE A LED	0	SIDE A LED ON/OFF. Basically (NC) only with compatible.	H:ON
11	P25	SIDE B LED	0	SIDE B LED ON/OFF. Basically (NC) only with compatible.	H:ON
12	P24	DVD illumination	0	DVD illumination lamp ON/OFF.	H:ON
13	P23	XRDY	0	Communications handshake line with system controller.	L: communications enabled
14	P22	SCK1	I/O	Communication clock output with system controller.	-
15	P21	SO1	I/O	Communication data output with system controller.	•
16	P20	SI1	I	Communication data input with system controller.	-
17	RESET	RESET IN	I	Reset input.	L: reset
18	P74	Condition LED	0	Condition OED ON/OFF.	L:ON
19	P73	Last memory LED	0	Last memory LED ON/OFF.	L:ON
20	AVss	Vss		•	
21	P17	POWER ON	0	SW5V ON/OFF.	H:ON
22	P16	RESET OUT	0	System reset output.	L: reset
23	P15	(NC)	0	-	-
24	P14	(NC)	0	•	-
25	P13	KIN1	I	Key input.	
26	P12	KIN0	I	Key input.	
27	P11	MS1	I	Destination determination input.	
28	P10	MS0	I	Destination determination input.	
29	AVdd	AVDD		-	•
30	AVREF	AVref	-	-	-
31	P04	P04	I	(Not used)	-
32	XT2	(NC)	-	-	-
33	Vss	Vss	I	-	
34	X1	X1	I	Microprocessor clock connection.	
35	X2	X2	-	Microprocessor clock connection.	
36	P37	(NC)	0		
37	P36	(NC)	0		
38	P35	(NC)	0	-	1-
39	P34	(NC)	0		
40	P33	(NC)	0		

# DVL-90, DVL-700

No.	Name	Function Name	1/0	Function	ACTIVE
41	P32	(NC)	0		
42	P31	(NC)	0		
43	P30	(NC)	0	-	-
44	P03	(NC)	0		
45	P02	(NC)	0		
46	P01	LT1	I	Communications handshake line with system controller.	L: communications enabled
47	P00 .	SELIR	I	Remote control signal input.	
48	IC	IC	ŀ	-	-
49	P72	(NC)	0		
50	P71	(NC)	0	-	-
51	P70	(NC)	0		
52	Vdd	VDD	-	-	-
53	P127	DISP LED	0	Display LED ON/OFF.	H:ON
54	P126	GUI LED	0	GUI LED ON/OFF.	H:ON
55	P125	(NC)	0		
56	P124	(NC)	0	-	-
57	P123	(NC)	0		
58	P122	S15	0		
59	P121	S14	0		
60	P120	S13	0	FL segment output.	H:ON
61		S12	0		
62	P116	S11	0		
63	P115	S10	0		
64	P114	(NC)	0	-	-
65	P113	(NC)	0	-	-
66		S9	0		
67	P111	S8	0		
68		S7	0	FL segment output.	H:ON
	P107	S6	0		
70	P106	S5	0		
71	Vload	-30V	-	Input for -30V.	
72	P105	S4	0		
	P104	S3	0	_	
1	P103	S2	0	FL segment output.	H:ON
75	P102	S1	0		
	P101	S0	0		
77	P100	T10	0		
78	P97	T9	0	FL segment output.	H:ON
79	P96	T8	0		
80	P95	<b>T</b> 7	0		

### ■ PD0246A2 (CLD MAIN ASSY : IC101)

### • LD MECHANISM CONTROL IC

### ● Pin Arrangement (Top View)

(1-ch)						-	
+5V	i	1 Vcc	1 1	P20/I/O	64	_ XANA	(O LI)
	_	1 Vcc 2 P67/O	لسا	P21/I/O	63	C XCX	(O,H)
	_	3 P66/O		P21/I/O	62	\$Q2	(O,L)
XPLAY (O,H)				P23/I/O	61		(O,H)
SCK3/XCQCK (O,H)		4 P65/O				SQ1	(O,H)
XCD (O,H)	_	5 P64/O		P24/I/O	60	- SRDMUTE	(O,H)
TILTERR (A/D)		6 P63/A/D 3		P25/I/O	59 58	WRQ	(1)
TBALERR (A/D)		7 P62/A/D 2		P26/I/O	57	- XFOK	(1)
SLDRERR (A/D)	_	8 P61/A/D 1		P27/I/O		- DETPOW	(1)
SLDRPOS (A/D)	_	9 P60/A/D 0		P00/I/O	56	XCLD_P.U_C	
FSEQ (I)	_	10 P47/I/O/INT4		P01/I/O	55	- XTURNA	(1)
CURRENT DET (1)	_	11 P46/I/O/INT3		P02/I/O	54	— XTURNB	(1)
TBALDRV (PWM,L)		12 P45/I/O/PWM2		P03/I/O	53	TILT SUM/DEF	
SHAKE (I/O,Z)	-	13 P44/I/O/DOCI		P04/I/O	52	- NROFF	(O,L)
RFCORR (O,L)	_	14 P43/I/O/MACS		P05/I/O	51	N.C.	(O,L)
SQOUT (I)	_	15 P42/I/O/SI2		P06/I/O	50	- DOCINH	(1)
COIN/SO3 (O,H)	_	16 P41/I/O/SO2		P07/I/O	49	— TZC SEL	(O,H)
CQCK/SCK3 (O,H)	-	17 P40/I/O/SCK2		P10/I/O	48	DVPLAT	(O,H)
SLDRDRV (PWM,Z)	_	18 P37/I/OPWM 1		P11/I/O	47	)— THOLD	(1)
SI1 (I)	_	19 P36/I/O/SI1		P12/I/O	46	— N.C.	(O,L)
SO1 (O,H)	_	20 P35/I/O/SO1		P13/I/O	45	N.C.	(O,L)
SCK1 (I/O)	_	21 P34/I/O/SCK1		P14/I/O	44	— N.C.	(O,L)
TZC (1)		22 P33/I/O/CNTR		P15/I/O	43	MEMLAT	(O,H)
SBSY (1)	-	23 P32/I/O/INT2		P16/I/O	42	I— WFM/VLOCK	(1)
TILTORY (I/O,Z)		24 P31/I/O		P17/I/O	41	D_EXT	(O,L)
TURNDRY (3 STATE,	<b>)</b>	25 P30/I/O		Vsync/I	40	XPBV	(1)
XPBV (I)	_	26 P50/INT1		Hsync/I	39	— XPBH	(1)
CNVSS		27 CNVss		DATA/I	38	DATA	(1)
XRESET		28 RESET		P53/I	37	— FG	(1)
XIN		29 Xin		P54/I	36	TBCLOCK	(1)
XOUT	_	30 Xou		P55/I	35	SW2	(i)
Φ	_	31 Ф		P56/I	34	— SW3	(1)
GND		32 Vss		P57/I	33	SW1	(i)
				. 0.77		l	٠.,

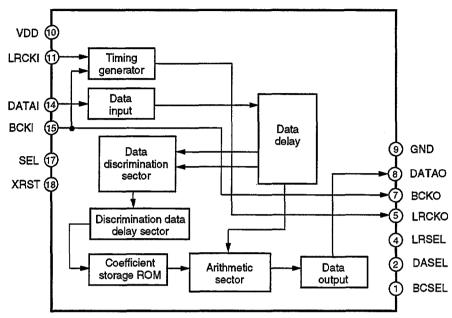
No.	Pin Name	1/0	Pin Function					
1	vcc	l	ower supply pin Apply 5V ± 10%					
2	RWC	0	DSP read/write command signal output "L"= Read "H"= Write					
3	XPLAY	0	Signal output during spindle servo "L"= During servo "H"= During acceleration, brake and stop					
4	sскз/хсоск	0	DVP/DSP clock switch "H"= DVP "L"= DSP					
5	XCD	0	LD/CD switch signal output "L= CD "H"= LD					
6	TILTERR	I A/D	This signal is A/D converted as the tilt servo control input. Control the tilt motor so that this signal becomes 2.5V.					
7	TBALERR	I A/D	Tracking balance error signal input This signal is A/D converted as the tracking offset control input.					
8	SLDERR	I A/D	This signal is A/D converted as the slider servo control input. Control the slider motor so that this signal becomes 2.5V.					
9	SLDPOS		Pickup position detection switch input Detect the position by reading A/D input value which each switches are resistance divided.					
10	FSEQ	ı	Subcode sync. confirmity detection signal input "L"= Not confirmity "H"= Confirmity					
11	CURRENTDET	1	Spindle over-current detection signal input "L" = Over current "H"= Normal					
12	TBALDRV	O PWM	Output the tracking offset signal to PWM output, then use for auto tracking offset. 910µsec period, tri-state control H, L, Z					
13	SHAKE	1/0	Handshake signal for data communication with the mode control IC This pin is the bilateral data line and each microprocessor control the Input/Output.					
14	RFCORR	0	RF correction switch signal output "H"= Gain UP CD, CDV-A:Low, CAV inner circuit gain up, others are High.					
15	SQOUT	1	Command data input from DSP Read out SUBQ					
16	SO3/COIN	0	Command data output to DVP/DSP					
17	SCK3/CQCK	0	DVP/DSP read/write command clock output Read-in at rising edge					
18	SLDDRV	O PWM	Slider control signal output 5V= FWD, 0V= REV, 2.5V= STOP 910µsec period, tri-state control H, L, Z					

No.	Pin Name	I/O	Pln Function					
19	SI1	1	Data input from the mode control IC					
	SO1	0	Serial data output to the mode control IC					
			lock for serial communication with the mode control IC					
21	SCK1	1/0	ecomes input mode without communicate with the mode control IC racking error zero cross signal input					
22	TZC	IINT	Monitor this signal when searching track count in the miss clamp detection					
23	SBSY	1	Subcode block sync. input					
24	TILTDRV	1/0	LOAD/TILT control output  0.5V= Tray IN, OUT/Tilt DOWN, UP 2.5V=STOP Use for tilt servo that tilt drive is PWM output.					
25	TURNDRV	0	Turn drive signal output					
26	XPBV	i	Playback vertical sync. signal input of LD/CDV "L"= During vertical sync.					
27	CNVSS	1	Ground for A/D conversion					
28	XRESET	ı	Reset signal input "L"= Reset "H"= Release reset Mode control IC is controlled.					
29	XIN	Ī	9MHz clock oscillation input					
30	XOUT	0	9MHz clock oscillation output					
31	N.C.	0	Not used					
32	GND	ı	Ground					
33	SW1							
34	SW3	ŀ	Switch input for Loading/Tilt position detection					
35	SW2							
36	TBCLOCK	1	Spindle lock signal input "L"= Unlock "H"= Lock					
37	FG		Spindle motor FG signal input 16 outputs per rotation Used after dividing by 2 in the microprocessor					
38	DATA	1	Input for Phillips code decoder with built-in mechanism controller					
39	XPBH	1	Playback H-SYNC input for Phillips code decoder					
40	XPBV		Playback V-SYNC input for Phillips code decoder					
	D_EXT	0	Control signal output for video dynamic extension "H"= ON "L"= OFF					
	WFM	<del>-</del>	Field discrimination signal from DVP "H"= ODD "L"= EVEN					
	MEMLAT	0	Serial control latch output of memory control IC PD3212A Latches at falling edge.					
	N.C.	<del>-</del>	Not used					
	N.C.	0	Not used					
	N.C.	<del>-</del>	Not used					
	THOLD	<del></del>	Track jump accelerating / decelerating signal input "L"= Other "H"= During accelerating / decelerating					
	DVPLAT	<u>,</u>	PD6159B serial latch signal output Latches at falling edge.					
	TZCSEL		TZC switch signal output "H"= at normal "L"= at CD/DVD disc discrimination					
	DOCINH	0	Control the clamp pulse and clamp killer by tri-state value					
	N.C.	<del>-</del>	Not used					
	NROFF	<del>-</del>	Noise reduction control output by VDEM "L"= Normal "H"= Not NR					
	TILT SUM		Disc present/absent detecting signal input by the tilt sum in the DVD P.U. mode "H"= Absent "L"= Present					
	XTURNB	1	Turn switch input "H"= Side A / turn "L"= Side B					
	XTURNA	1	Turn switch input "H"= Side B / turn "L"= Side A					
	XLDPUCUT	1	LD P.U. out position detecting switch input "H"= LD P.U. active "L"= LD P.U. out position					
	DETPOW	1	Use for power abnormal signal input port "L"= Normal "H"= Abnormal					
	XFOK	<u> </u>	Focus servo lock signal input "L"= Lock "H"= Unlock Use for lock detection of focus servo					
	WRQ	<u> </u>	Subcode Q reading OK signal input "L"= NG "H"= OK					
	SRDMUTE	0	This pin will be H when subcode Q data passed by CRC check.  Mute control signal output for AC3 Release MUTE during playback. "L"= Release MUTE "H"= MUTE					
	SQ1	<del>-</del>	Analog audio switching signal output 1/L "L"= Squelch OFF "H"= Squelch ON					
	SQ2	<del>-</del>	Analog audio switching signal output 2/R "L"= Squelch OFF "H"= Squelch ON					
	XCX	<del>-</del>	Analog audio CX noise reduction switching signal output "L"= CX ON "H"= CX OFF					
	XANA		Digital / Analog audio switching signal output "L"= Analog "H"= Digital					
<u> </u>	/\/\\\\\		Prigram, many again santring signal output E-miany II-Digital					

### **■ PD0236AM (CLD MAIN ASSY : IC202)**

### • HI-BIT IC

### Block Diagram



No.	Pin Name	1/0	Pin Function
1	BCSEL	lp	fs selection of bit clock (built-in pull-up) H: BCKI = 48fs , L: BCKI = 64fs
2	DASEL	lp	Output data length selection when the bit length expansion function is ON. H:DATAO = 20 bit, L:DATAO = 24 bit
3	(NC)	-	Not used (Open or VDD)
4	LRSEL	<b>l</b> p	LRCKO polarity selection (built-in pull- <u>up)</u> H : LRCKI = LRCKO ,L : LRCKI = LRCKO
5	LRCKO	0	LR clock output
6	(NC)	_	Not used (Open or VDD)
7	вско	0	Bit clock output
8	DATAO	0	Data output
9	GND	_	Ground pin
10	VDD		Power supply pin
11	LRCKI	1	LR clock input
12	(NC)	-	Not used (Open or VDD)
13	(NC)	_	Not used (Open or VDD)
14	DATAI	1	Data input
15	BCKI	I	Bit clock input
16	(NC)	_	Not used (Open or VDD)
17	SEL	lp	Bit length expansion process / input data output selection (built-in pull-up) H :Expansion process (output word length : 20/24 bit), L : Input data output
18	XRST	1	Reset pin H: Normal, L: Reset

### ■ HD6417032F20 (DVD MAIN ASSY : IC101)

 $\bullet$  SYSTEM  $\mu$ - COM

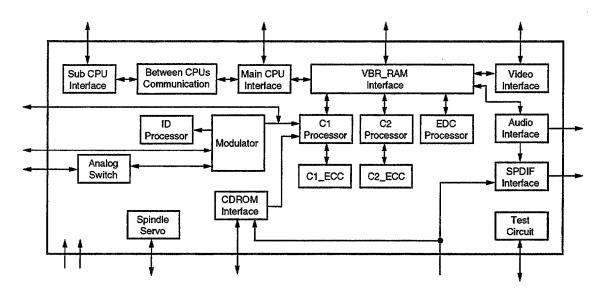
No.	in Functi Name	Signal Name	I/O	Active	Function
1	XIRQ6	XIRQ6	I	L	Interrupt input from LSI-1.
2	XIRQ7	XIRQ7	I	L	Interrupt input from µPD61020.
3	Vss	Vss	-	-	Grounding.
4	AD0	AD0	I/O	-	Crounding.
5	AD1	AD1	1/0		
6	AD2	AD2	I/O	<u> </u>	1
7	AD3	AD3	1/0	<del></del>	Data bus.
8	AD4	AD4	I/O	-	
9	AD5	AD5	1/0	-	1
10	AD6	AD6	I/O	-	
11	AD7	AD7	ΙΟ	-	
12	Vss	Vss	-	-	Grounding.
13	AD8	AD8	I/O	-	Data bus.
14	AD9	AD9	I/O	-	Data bus.
15	Vcc	Vcc	-	-	Power supply.
16	AD10	AD10	I/O	•	
17	AD11	AD11	I/O	-	_
18	AD12	AD12	I/O	-	Data bus.
19	AD13	AD13	I/O	-	
20	AD14	AD14	I/O	-	
21	AD15	AD15	1/0	-	
22	Vss	Vss	-	•	Grounding.
23		A0 (XHBS)	0	-	
24	A1	A1	0	-	
25	A2	A2	0	-	
26	A3	A3	0	-	Address bus.
27	A4	A4	0	-	
28	A5	A5	0	-	
29	A6	A6	L	-	
30	A7	A7	0		Complete
31	Vss A8	Vss A8	- 0	<u>-</u>	Grounding.
33	A9	A9	0		-
34	A10	A10	0	-	
35	A11	A11	0	<del></del>	Address bus.
36	A12	A12	0		Addition bus.
37	A13	A13	0		
	A14	A14	0	<u> </u>	
39	A15	A15	0	-	
40	Vss	Vss	-	-	Grounding.
41	A16	A16	0	•	Address bus.
42	A17	A17	0	-	Address bus.
43	Vcc	Vcc	-	-	Power supply.
44	A18	A18	0	•	
45	A19	A19	0	-	Address bus.
46	A20	A20	0	•	
47	A21	A21	0	-	
	XCS0	XCS0	0	L	Chip selection to program ROM.
	XCS1	XCS1	0	L	Chip selection to work SRAM.
	XCS2	XCS2	0	L	Chip selection to GUI-ROM.
	XCS3	XCS3	0	L	Chip selection to LSI-1.
	Vss	Vss	-	-	Grounding.
	XCS4	XCS4	0	L	Chip selection to LSI-2.
	XCS5	XCS5	-	-	Not used.
	XCS6	XCS6	0	L	Chip selection to µPD61020.
56	XWAIT	XWAIT	I	L	Weight input for bus cycle.

No.	Name	Signal Name	ľO	Active	Function
57	XWR	XWR	0	L	Signal for external write.
58	PA5	PA5	0	-	TP58 (test pin).
59	XRD	XRD	0	L	Signal for external read.
60	PA7	XLT3	0	L	Latch signal to PD2026/29.
61	Vss	Vss	_	-	Grounding.
62	PA8	XLT2	0	L	Latch signal to ZR38521.
63	PA9	XDAKE	0	L	LSI-1 and LSI-2 direct DMA enable output.
64	TIOCA1	XQ2	I	L	Interrupt input from LSI-2.
65	PA11	LTI	0	Н	Handshake output to FL CON.
66	DACK0	DACK0	0	н	Signal to acknowledge request for DMA transfer to LSI-1.
67	XDREQ0	XDREQ0	I	L	Signal to acknowledge request for DMA transfer from LSI-1.
68	DACK1	DACK1	0	L	Signal to acknowledge request for DMA transfer to LSI-2.
69	XDREQ1	XDREQ1	I	L	Signal to acknowledge request for DMA transfer from LSI-2.
70	Vcc	Vcc		_	Power supply.
71	CK	CK	0		System control clock output. Not used.
72	Vss	Vss	-	_	Grounding.
73	EXTAL	EXTAL	I		Crystal oscillator input.
74	XTAL	XTAL	Ī	-	Crystal oscillator input.
75	Vcc	Vcc	_		Power supply.
76	NMI	NMI	I		NMI input (pull-up). Not used.
77	Vcc	Vcc			Power supply.
78	XWDTOF	WDTOF	0	L	Watchdog timer output. Not used.
79	XRES	XRES	I	L	Reset input.
80	MD0	MD0	Ī	- <u>-</u>	Operation mode setting terminal (H).
81	MD1	MD1	I		Operation mode setting terminal (L). Set to Mode 1.
82	MD2	MD2	I		Operation mode setting terminal (L). Set to Wode 1.
83	Vcc	Vcc	_		Power supply.
84	Vcc	Vcc			Power supply.
85	AVcc	AVcc	I I		Analog power supply.
86	AVcc	AVref			Analog reference voltage input.
87	ANO	ANO			Analog signal input (pull-up). Not used.
88	AN1	AN1	I	-	Analog signal input (pull-up). Not used.
89	AN2	AN2	I	<u>-</u>	Audio level (Lch) input.
90	AN3	AN3	I	-	Audio level (Cch) input.  Audio level (Rch) input.
91	AVss	AVss		-	Analog power grounding.
92	PC4	XSDET		-	Sync detection input.
93	PC5	XSEL2	I	-	Test mode determination input.
94	PC6	CDGM	I	H	Graphic input data detection input.
95	PC7	CTS	I	H	CTS (for RS-232).
96	Vss	Vss	_		Grounding.
	PB0	FMATT	0	-	LD FM audio attenuation output.
98	PB1	BSEL	0	•	Hi Bit clock selection output.
	Vcc	Vcc	-	-	Power supply.
	TIOCA3	HIBSEL	0	-	Hi Bit expansion selection output.
	PB3	XIRQCDROM	I	-	Interrupt input from CDROM decoder.
	PB4	XRDY	I	L	Ready signal input from FL microprocessor.
	PB5	DTR	0	-	DTR output (for RS-232).
	PB6	GCS	Ö	Н	Chip selection for CDG.
-	PB7	DPSEL	0		Optical output selection output. PCM/AC3.
-	Vss	Vss	-	_	Grounding.
	RxD0	SSI	I	-	Serial IN (synchronizing the clock).
	TxD0	SSO	0	-	Serial OUT (synchronizing the clock).
	RxD1	RXD	Ī	-	Serial IN (synchronizing adjustment).
-	TxD1	TXD	0		Serial OUT (synchronizing adjustment).
	SCK0	SSCK	I/O		Serial clock input/output (synchronizing the clock).
	XIRQ5	XQ10	I	L	Interrupt input from LSI-1 INT1.
			•		

### **■ PD4695A (DVD MAIN ASSY : IC161)**

• DVD DECODER

### Block Diagram



No.	Pin Name	1/0	Pin Function			
1	GND		Ground for digital circuit			
2	GND		Ground for digital circuit			
3	DXTLO	0	Connect a 27MHz crystal which is oscillated PLL reference clock			
4	DXTLI	ı	When input a signal from the external, connect to DXTLI.			
5	VDD	-	Power supply for digital circuit Connect to +5V.			
6	PEQL	ı	Not used Fixed to GND or VDD.			
7	PEQH	ı	Not used in linea to diffe of VDD.			
8	SELNED	1	Set the input/output direction of NED (7:0), STB and BSYNC pins 0 for input.			
9	STB	1/0	Strobe signal which is indicated data of after the 8/16 demodulation is in NED (7:0) pins			
10	BSYNC	1/0	Pulse which is indicated the lead of ECC block			
11	NED7					
	NED6	1/0	B bit parallel data input/output of after the 8/16 demodulation			
13	NED5	"				
	NED4					
	VDD	_	Power supply for digital circuit Connect to +5V.			
	GND		Ground for digital circuit			
	NED3					
	NED2	1/0	8 bit parallel data input/output of after the 8/16 demodulation			
	NED1		is parametriance improvement of another or to administration			
	NED0					
	DD7					
22	DD6					
23	DD5	1/0	DRAM data bus for VBR buffer			
24	DD4					
	DD3					
26	GND	_	Ground for digital circuit			

No.	Pin Name	1/0	Pin Function									
27	VDD		Power supply for digital circuit Connect to +5V.									
ļ	DD2		- the supply for algues should both both of the									
	DD1	1/0	DRAM data bus for VBR buffer									
	DD0											
	XDRAS	0	DRAM RAS signal of VBR buffer									
ļ	XDCAS	0	DRAM CAS signal of VBR buffer									
	XDOE	<del>-</del>	DRAM OE signal of VBR buffer									
<u> </u>	XDWE	0	DRAM WE signal of VBR buffer									
L	DA10											
	DA9											
	DA8	0	DRAM address signal for VBR buffer									
L	DA7	_										
	DA6											
40	GND		Ground for digital circuit									
	VDD	_	Power supply for digital circuit Connect to +5V.									
	DA5											
	DA4											
	DA3	_										
	DA2	0	DRAM address signal for VBR buffer									
46	DA1											
47	DAO											
48	SREQ	ı	Data transfer request pin from the MPEG decoder									
49	XWR											
50	XSACK	0	Data transfer response pin to the MPEG decoder Output form is changed by setting.  Ground for digital circuit									
51	GND											
52	GND	_	nound for digital circuit									
53	VDD	_	Power supply for digital circuit Connect to +5V.									
54	SDATA0											
55	SDATA1	0	Data output hus to the MPEG decoder									
56	SDATA2	U	Data output bus to the MPEG decoder									
57	SDATA3											
58	GND	_	Ground for digital circuit									
59	VDD	_	Power supply for digital circuit Connect to +5V.									
60	SDATA4											
61	SDATA5	0	Data output bus to the MPEG decoder									
	SDATA6	-										
	SDATA7											
-	LSYNC	0	Line sync. detecting output in the demodulator									
	DMACKI	ı	System clock input of DVD and CD ROM decoder Input 10 to 29MHz.									
	GND		Ground for digital circuit									
	DMCKO	0	Outputs a clock which is oscillated and input at DXTLI and DXTLO pins Normally, connect to DMACKI.									
68	XSCL1	<u> </u>	Chip select signal from the main CPU When this signal is Low, XSRD/XSWR becomes effectively.									
	XSWAIT	0	WAIT output against to the main CPU When this pin is Low, you should not stop the access from the main CPU. This pin is open-drain.									
	XSRD	ı	Connect to RD signal of main CPU									
	XSWR	ı	Connect to WR signal of main CPU									
	XSDREQ	0	DMA request against to the main CPU Drive the DMA transfer at Low level or falling edge.									
$\vdash$	SDACK	ı	DMA response signal When this signal is High, outputs the data to SAD (7:0).									
	XSDREQ2		Connect the DMA request signal of other device.									
$\vdash$	SA6											
	SA5	ı	Connect the address bus of the main CPU									
77	SA4											

No.	Din 11	I/O	Pin Function								
70	Pin Name										
	VDD		Power supply for digital circuit Connedct to +5V.								
	GND		Ground for digital circuit								
	SA3										
	SA2	ı	Connect the address bus of the main CPU								
	SA1										
	SA0										
	SOUTH	<u> </u>	Serial output which is used the DMA channel of CPU Outputs the upper nibble.								
	SAD7										
	SAD6	1/0	Connect the data bus of the main CPU								
	SAD5		Minest the data bus of the main of o								
	SAD4										
89	VDD		Power supply for digital circuit Connedct to +5V.								
90	GND		Ground for digital circuit								
91	SAD3										
92	SAD2	1/0	Connect the data bus of the main CPU								
93	SAD1		onness are data and or the main of o								
94	SAD0										
95	DUTY50	0	Always outputs the duty 50% pulse Apply the reference voltage of each PWM signal of demodulation system.								
96	XIRQ10	0	Low for require the interrupt against to the main CPU Setable the output pins with the register.								
97	XIRQ11	J	Low for require the interrupt against to the main one of Setable the output pins with the register.								
98	TSTSTB	ı	Set the LSI to operate the test mode Test mode for High input.								
99	BMODE0										
100	BMODE1		Set to perform the any test in the test mode								
101	BMODE2	ı	ser to benoun me and rear in me rear mode								
102	BMODE3										
103	BUNRI	ı	Separation test control pin of the internal RAM Inputs Low in the actual use.								
104	VDD	-	Power supply for digital circuit Connedct to +5V.								
105	GND		Cround for digital signifit								
106	GND	-	tround for digital circuit								
107	AXTLO	0	36.864MHz or 24.576MHz crystal connect pin which is oscillated the reference clock to use the audio output circuit.								
108	AXTLI	Ī	When input a signal from the external, connect to AXTLI.								
109	VDD		Power supply for digital circuit Connedct to +5V.								
110	CKCD	I	Reference clock of CD audio output Inputs 16.9MHz.								
111	GND	-	Ground for digital circuit								
112	PV		When the master clock is AV synchronized, outputs the pulse which is frequency divided the audio side clock (AXTLI input) for apply to the PLL circuit.								
113	PREF		When the master clock is AV synchronized, outputs the pulse which is frequency divided the video side clock (DMACKI input) for apply to the PLL circuit.								
114	скоит	0	Frequency divided signal which is connected to AXTL pin and use for DAC control Frequency is changed by the mode.								
115	вск	0	Bit clock output to DAC and audio decoder It is 48fs or 64fs of the source.								
116	LRCK	0	LRCK signal output to DAC and audio decoder								
117	ADATA0	0	Outputs the compression data when source is AC3/MPEG and outputs CH0/CH1 when source is linear.								
118	ADATA1										
119	ADATA2	0	Output CH2/CH3 when source is linear								
120	ADATA3										
121	SBUSY	ı	Busy signal for output control the serial output of SOUTL, SOUTH pins								
122	DIFOUTO	0	Digital output by switching the compression data and linear data When linear data is output, output the same as that of the DIFOUT1.								
123	DIFOUT1	0	Digital out for linear data only Outputs CH0&CH1/AC3/MPEG/CD of DVD linear correspond to the source.								
	VALID	0	When source is AC3/MPEG, it becomes High level during effective data output								
124			·								

N <sub>2</sub>	Pin Name	VO	Pin Function
No.	1		
	CDBCK	1	Bit clock input from the CD decoder Expect frequency is 2.1168MHz (48fs).
	CDLR	<u> </u>	LRCK signal input from the CD decoder
	CDDT	1	Audio data input from the CD decoder
	CDDO	ı	Digital output signal input from the CD decoder Outputs by switching it of DVD into LSI.
	VDD		Power supply for digital circuit Connect to +5V.
	GND		Ground for digital circuit
132	WFCK	ı	CD frame clock signal Connect to same pin name pin of the CD decoder IC.
133	SCOR	<u> </u>	CD subcode sync. input Connect to same pin name pin of the CD decoder IC.
134	SBSO	l	CD subcode data input Connect to same pin name pin of the CD decoder IC.
135	EXCK	0	Shift clock to making the timing of data transfer to SBSO pin
136	SOUTL	0	Serial output which is used the DMA channel of CPU and outputs the lower nibble
137	ASTB	ı	Strobe signal which is indicated the address information in MAD (7:0) Connect to ASTB of sub CPU.
138	XMCS	1	Chip select signal from the sub CPU When this signal is Low, XMRD/XMWR will be effective.
139	XIRQ2	l	Low for require the interrupt against to the sub CPU
140	XMWR	ı	Connect to WR signal of the sub CPU
141	XMRD	Ī	Connect to RD signal of the sub CPU
142	MAD7		
143	MAD6		
144	MAD5	1/0	Connect to multiplex bus of address data of the sub CPU
145	MAD4		
146	VDD	_	Power supply for digital circuit Connect to +5V.
-	GND	_	Ground for digital circuit
	MAD3		
	MAD2		
	MAD1	1/0	Connect to multiplex bus of address data of the sub CPU
	MADO		
152			
153			
154			
	GND		
	GND	_	Ground for digital circuit
157			Power supply for digital circuit Connect to +5V.
<u> </u>	XRESET	1	Initialize the whole LSI system by Low level input
	FGPL	i	Rotation pulse input from the spindle motor
	RFA	1	External binary RF signal input for the rough servo Connect to GND at not used.
	FPWM	· ·	7 bit PWM output for the FG servo Tri-state output of High, Low and Hi-impedance
162			Rotaion direction of the spindle motor indicating output
	VPWM	<del>-</del>	5 bit PWM output for the velocity servo Tri-state output of High, Low and Hi-impedance
$\vdash$	GND	_	Ground for digital circuit
	VDD		Power supply for digital circuit Connect to +5V.
	PPWM		PWM output for the phase servo Tri-state output of High, Low and Hi-impedance
	RPWM	0	4 bit PWM output for the rough servo Tri-state output of High, Low and Hi-impedance
	RERR	0	Control pin for the rough servo Tri-state output of High, Low and Hi-impedance
	PLRE		RRPW pin output without tri-state control
	LOCAL	<del>-</del>	Input for local operaion of the demodulation system
	SCLK	0	Clock pulse output with synchronizing the main data after the 8/16 demodulation
			Test signal to connect the error measuring instrument
	SDATA	0	Serial output the main data after the 8/16 demodulation Test signal to connect the error measuring instrument
	SEDI	<u> </u>	Serial data input after the ビタビ複号 Normally, connect to SEDO pin.
	SEDO	0	Serial data output after the ビタビ複号 Normally, connect to SEDI pin.
175	GND		Ground for digital circuit

# DVL-90, DVL-700

No.	Pin Name	I/O	Pin Function
176	VCOCLK	l	System clock of the spindle demodulator Connect to the external VCO.
177	SLIP	0	When PLL cycle slip is occured, outputs the pulse of prescribed width.
178	APC	0	Phase difference of PLL outputs as PWM pulse
179	ATC	0	DC difference of RF signal outputs as PWM pulse
180	AFC	0	Frequency difference of PLL outputs as PWM pulse
181	DOC	0	When the polarity of RF signal is not turned more than 32 clocks, it is supposed to drop out then output the flag.
182	GND	_	Ground for digital circuit
183	VDD	_	Power supply for digital circuit Connect to +5V.
184	,		
185	AVDD		Power supply for analog circuit Connect to +5V.
186	AINO	i	Analog switch input/output for controling the amplitude of RF signal
187	AOUTO	0	Analog switch is ON/OFF correspond to the amplitude of RF signal
188		· · · · · · · · · · · · · · · · · · ·	
189	AIN1	1	Analog switch input/output for controling the amplitude of RF signal
190	AOUT1	0	Analog switch is ON/OFF correspond to the amplitude of RF signal
191			
192			
193	AIN2		Analog switch input/output for controling the amplitude of RF signal
194	AOUT2	0	Analog switch is ON/OFF correspond to the amplitude of RF signal
195			
196			
197	AIN3	ı	Analog switch input/output for controling the amplitude of RF signal
198	AOUT3	0	Analog switch is ON/OFF correspond to the amplitude of RF signal
199	AGND		Ground for analog circuit
200	ADD0		
201	ADD1		
202	ADD2	ı	
203	ADD3		Input RF sampling value after the A/D conversion to 8 bit parallel data
204	ADD4	,	Imput nr sampling value and the AVD conversion to a bit paramet data
205	ADD5		
206	ADD6	:	
207	ADD7		
208	VDD	_	Power supply for digital circuit Connect to +5V.

### ■ HM514800CJ-7 (DVD MAIN ASSY: IC162)

### • 4M DRAM

No.	Pin Name	Pin Function					
1	Vcc	Power supply					
2	1/00						
3	1/01	Data input/output					
4	1/02	Data inputourput					
5	1/03						
6	NC	Non connection					
7	WE	Read/Write enable					
8	RAS	Low address strobe					
9	A9						
10	A0						
11	A1	Address input/Refresh address input					
12	A2						
13	A3						
14	Vcc	Power supply					
15	Vss	Ground					
16	A4						
17	A5						
18	A6	Address input/Refresh address input					
19	A7						
20	A8						
21	NC	Non connection					
22	OE	Output enable					
23	CAS	Column address strobe					
24	1/04						
25	1/05	Data innut/authurt					
26	I/O6	Data input/output					
27	1/07						
28	Vss	Ground					

### ■ PD4784A (DVD MAIN ASSY : IC201)

• MECHANISM CONTROL IC

### • Pin Assignment

	← FDMON	← LDS_ERR	← FCS_ERR	← SLD_POS	+ LOD_POS			← DEFECT						◆ SHAKE	<b>←</b> SENS	◆ scor	← RFCK	← FZC	← XIRQ2	<b>→</b> TZC			
	ANI4	ANI3	ANIZ	ANI1	ANIO		Ī	Ę						NTP6	INTPS	NTP4	INTP3	NTP2	INTP1	INTPO			
Г						75: 7 AVREFO A	74:		72: XT2	71: IC	70: X1	69: X2	68: Voc						62: P01	61: P00	7		
LD_ON - ANIS						Å	Voo '									. • .				RESET:60	,		
SRD_ON ← ANI6	2:P16																			P127:59	RTP7	->	F_RESET
12/X8 ← ANI7	3:P17																			P126:58	RTP6	->	SWPDIR
4	4:AVss																			P125:57	RTP5	-	OEIC_G
ATB_DRV ← ANO0	5:P130																			P124:56	RTP4	-	FBAL_ON
RF_BIAS ← ANO1	6:P131																			P123:55	RTP3	->	FSHUNT
	7:AVREF1																			P122:54	RTP2	<b>→</b>	FK-
LDM_SO → SI2 8	8:P <b>7</b> 0							<b>y</b>	_	4 ===	_									P121:53	RTP1	*	FK+
LDM_SI - SO2	9:P71							H	עי	47	84	·A								P120:52	RTP0	<b>*</b>	F_JUMP
LDM_SCK ← SCK2	10:P72								т,	<b>~</b> D 1		A.								P37:51		<b>→</b>	T_OFF
SENS → SI1	11:P20								К	OP '	VIE'	VV								P36:50	BUZ	<b>→</b>	XPLAY
DATA - SO1	12:P21																			P35:49	PCL.	4	THLD
XCLOCK(SCLIQ*2 ← SCK1	13:P22																			P34:48	T12	4	DVDXCD
XLAT ←	14:P23																			P33:47	TI1	4	FSLICE
MUTE ◀	15:P24																			P32:46	TO2	4	AC3_TMP
saso -> sio	16:P25																			P31:45	TO1	4	
<b>←</b> soo	17:P26																			P30:44	T00	3	LOADDRV
SQCK ← SCK0	18:P27																			P57:43	ASTB	->	ASTB
ADO ← ADO	19:P40																			P66:42	XWAIT	->	ATB_ON
AD1 ◀ AD1																				P65:41	XWR	-	XWR
	P42 21:	P43 22:	P44 23:	P45 24:	P46 25:	P47 F 26: 2	250 I	P51 28:		P53 30:		P55 32:	Vss 33:	P56 34:		P60 36:	P61 37:	P62 38:	P63 39:	P64 40:			
	AD2	AD3	AD4	ADS	AD6	AD7	8	89	A10	A11	A12	A13		A14	A15	Ť.	F		F	CFIX			
	<b>\psi</b>	+	¥	+	+		¥	¥	¥	+	+	4		¥	+	<b>†</b>	¥	<b>↑</b>	<b>^</b>	<b>→</b>			
	AD2	AD3	AD4	ADS	AD6	AD7	A8	A9	A10	A11	A12	A13		A14	A15	TRDLMT	CLD	FOK	DVDPPK	XRD			

<sup>\*1</sup> Sets to open drain output during output.

<sup>\*2</sup> Connect to the XCLOC and SCLK terminals of CXD2545Q.

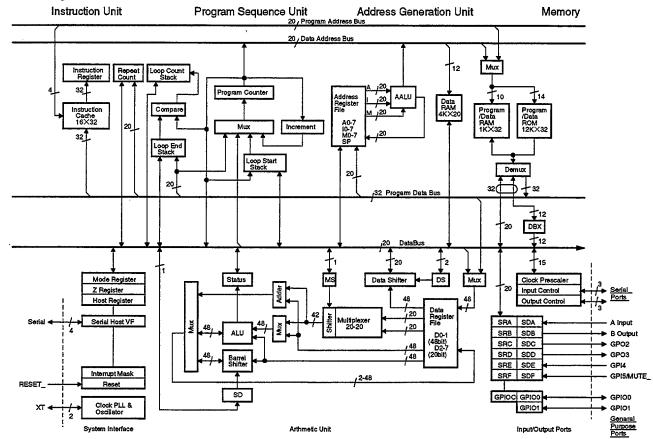
No.	Name	I/O	Function
1	LD_ON	OUT	Laser diode ON signal. H: active
2	SRD_ON	OUT	Switches command clock inhibit during serial read out. H: inhibit
3	12/X8.	OUT	DVD 8/12 cm switching signal.
4	AVss	-	Analog Ground.
5	ATB_DRV	D/A	ATB drive.
6	RF_BIAS	D/A	RD BIAS drive.
7	AVref1	-	Analog Reference Voltage 1.
8	LDM_SO	Serial I	LD mechanical controller communications data IN (SD ← LD).
9	LDM_SI	Serial O	LD mechanical controller communications data OUT (SD → LD).
10	LDM_SCK	Serial O	LD mechanical controller communications data CLOCK (SD ← LD).
11	SENS	Serial I	CXD2545Q Serial Read Out function output data input.
12	DATA	Serial O	CXD2545Q command data output.
13	XCLOCK (SCLK)	Serial O	Clock for CXD2545Q command/serial read out function.
14	XLAT	OUT	CXD2545Q LATCH signal.
15	MUTE	OUT	Power ON MUTE signal.
16	SQSO	Serial I	CXD2545Q SubQ data input.
17	NC.	OUT	Available.
18	SQSK	Serial O	Clock for CXD2545Q SubQ.
19	AD0	IO	
20	AD1	IO	
21	AD2	IO	
22	AD3	IO	Address/Data Bus.
23	AD4	Ю	
24	AD5	Ю	
25	AD6	IO	
26	AD7	Ю	
27	A8	OUT	
28	A9	OUT	
29	A10	OUT	Address Bus.
30	A11	OUT	
31	A12	OUT	
32	A13	OUT	
33	Vss	-	Ground.
34	A14	Expansion IO	Address Bus.
35	A15	Expansion IO	Address Bus.
36	TRDLMT.	IN	Tracking drive limit current detection signal input.
37	CLD	IN	Signal to control whether the pick of DVD or CD is active (Used with CLD compatible.).
38	FOK	IN	Focus OK signal.
39	DVDPRK	IN	DVD slider park IN signal (Used with CLD compatible.).
40	XRD	OUT	Read Strobe.

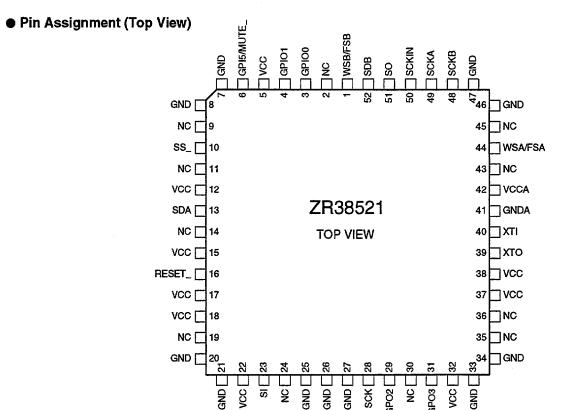
No.	Name	I/O	Function
41	XWR	OUT	Write Strobe.
42	ATB_ON	OUT	For ATB circuit ON/OFF.
43	ASTB	OUT	Address Strobe.
44	LOAD DRV	OUT	Loading drive.
45	NC.	OUT	Available.
46	AC3_TMP.	OUT	Signal for controlling AC3.
47	NC.	OUT	Available.
48	DVD/XCD	OUT	DVD/CD change-over SW (H: DVD, L: CD). The switch switches spindle error signal, etc.
49	THLD	OUT	Tracking hold signal ("H" duing jump).
50	XPLAY	OUT	For off-track measure circuit.
51	T_OFF		
52	F_JUMP	OUT	Focus jump switching signal ("H" during jump).
53	FK+	OUT	Focus jump kick pulse (+).
54	FK-	OUT	Focus jump kick pulse (-).
55	FCHUNT	OUT	Focus SHUNT SW control.
56	FBAL_ON	OUT	Focus Balance circuit control signal.
57	OEIC_G	OUT	OEIC GAIN SW switching signal.
58	SWPDIR	OUT	Sweep direction control.
59	GAIN_JDGE	OUT	Signal for disc judgment.
59	F_RESET	OUT	Peak hold reset signal for focus S.
60	XRESET	•	Mechanical controller hardware reset signal.
61	TZC	IN	TZC input.
62	XIRQ	IN	LSI1 interrupt (DVD-ID, system controller communications, FG-spindle).
63	FZC	IN	FZC interrupt (focus jump).
64	RFCK	IN	RFCK interrupt (error rate measurement).
65	SCOR	IN	SCOR interrupt (SubQ).
66	SENS	IN	SENS interrupt (fine search/MTJ) SENS monitor.
67	SHAKE	1/0	SHAKE interrupt input/SHAKE output (LD mechanical controller communications when CLD compatible is used).
68	Vdd	*	Power Supply (+5V).
69	X2	-	Cristal (Main System Clock).
70	X1	-	Cristal (Main System Clock).
71	IC	-	Internally Connected.
72	XT2	-	Crystal (Sub System Clock) ← Clock.
73	DEFECT	IN	DETECT signal input.
74	AVdd	•	Analog Power Supply.
75	AVref0	-	Analog Refernce Voltage0.
76	LOAD_POS	A/D	Loading SW read signal.
77	SLD_POS	A/D	Slider SW read signal.
78	FCS_ERR	A/D	Focus error signal.
79	LDSLDERR	A/D	SLD error input of LD pick-up (when compatible is used).
80	FDMON	A/D	A/D input signal for disc judgment.

### **ZR38521 (DVD MAIN ASSY : IC301)**

• AC-3 AUDIO DECODER

### Block Diagram





### **DVL-90, DVL-700**

### Pin Function

No.	Name	I/O	Function
1	WSB/FSB	I/O	Word selection or frame synchronous input/output for B Group serial port.
2	NC	1 .	Not used.
3	GPIO0	I/O	General-purpose I/O pin.
4	GPIO1	1/0	General-purpose I/O pin.
5	VCC	P	Power pin.
6	GPI5/MUTE	I	General-purpose input/mute pin.
7	GND GND	P P	GND pin.
8	GND	P	
<u></u>	<u> </u>	<del> </del>	GND pin.
9	NC		Not used.
10	SS_	I	Serial port interface: slave selection input (SPI).
11	NC	ļ <u>.</u>	Not used.
12	VCC	P	Power pin.
13	SDA	I	Data input for serial port A.
14	NC		Not used.
15	VCC	P	Power pin.
16	RESET_	I	Reset input.
17	VCC	P	Power pin.
18	VCC	P	Power pin.
19	NC	<u> </u>	Not used.
20	GND	P	GND pin.
21	GND	P	GND pin.
22	VCC	P	Power pin.
23	SI	I	Serial port interface: serial data input (SPI).
24	NC	-	Not used.
25	GND	I	GND pin.
26	GND	I	GND pin.
27	GND	P	GND pin.
28	SCK	I	Serial port interface: clock input (SPI).
29	GPO2	0	General-purpose output pin.
30	NC	-	Not used.
31	GPO3	0	General-purpose output pin.
32	VCC	P	Power pin.
33	GND	P	GND pin.
34	GND	P	GND pin.
35	NC	-	Not used.
36	NC	-	Not used.
37	VCC	P	Power pin.
38	VCC	P	Power pin.
39	XTO	0	Crystal oscillator output terminal.
40	XTI	I	Crystal oscillator input terminal.
41	GNDA	P	GND pin.
42	VCCA	P	Power pin.
43	NC	-	Not used.
44	WSA/FSA	I/O	Word selection or frame synchronous input/output for A Group serial port (for input).
45	NC	-	Not used.
46	GND	P	GND pin.
47	GND	P	GND pin.
48	SCKB	I/O	Clock input/output for B Group serial port.
49	SCKA	I/O	Clock input/output for A Group serial port.
	SCKIN	I/O	Clock input/output for B Group serial port.
	SO	0	Serial port interface: serial data output (SPI).
	SDB	0	Data input for serial port B.
		L	l i i

### Note:

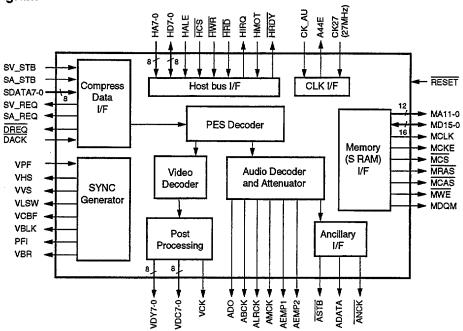
<sup>1)</sup> Connect an input terminal not to be used (TYPE = I) to VCC if active Low, or to GND if active High.

<sup>2)</sup> Do not connect output not to be used (TYPE = O), try state (TYPE = T), and NC terminal.

# ■ UPD61021 (DVD MAIN ASSY: IC401)

• MPEG2 DECODER

## Block Diagram



No.	Pin Name	ľO	Pin Function	No.	Pin Name	1/0	Pin Function
1	MD7	1/0	Data bus for 16 bit memory interface	21	GND	-	Ground pin
2	MD6	,	out 200 in to be money indicate	22	MD9	1/0	Data bus for 16 bit memory interface
3	GND	1	Ground pin	23	MD8	1/0	Data bus for 16 bit memory interrace
4	MD5	1/0	Data bus for 16 bit memory interface	24	VDD	-	Power supply pin
5	MD4		Data Due to To Sk montory menade	25	MDQM	0	Mask enable output signal of data input / output
6	VDD	ı	Power supply pin	26	MCLK	0	81MHz system clock output for memory
7	MD3	1/0	Data bus for 16 bit memory interface	27	мске	0	Clock enable output signal
8	MD2	1/0		28	GND	-	Ground pin
9	GND	-	Ground pin	29	CK27	ı	27MHz master clock input
10	MD1	1/0	Data bus for 16 bit memory interface	30	TCK81	ı	Test clock pin Input 81MHz. Connect to GND in the actual use.
11	MD0			31	VDD	_	Power supply pin
12	VDD	1	Power supply pin	32	T_RESET	ı	Test reset pin Connect to GND in the actual use.
13	MD15	1/0	Data bus for 16 bit memory interface	33	GND	-	Ground pin
14	MD14		Data suc 16. To Six monaco	34	T_PLL	I	PLL test input pin Connect to GND in the normal use.
15	GND	ı	Ground pin	35	TPH0	0	Test output pin
16	MD13	1/0	Data bus for 16 bit memory interface	36	YPH1		Open in the actual use.
17	MD12	120	Data bus for 10 bit memory interface	37	VDD	-	Power supply pin
18	VDD	1	Power supply pin	38	VPF	ı	Freeze signal Input when freezing the picture. Freeze is able to performed by the software command.
19	MD11	1/0	Data bus for 16 bit memory interface	39	VFI	0	Field index signal output Discriminate the output picture data is ODD or EVEN.
20	MD10			40	VBR	0	Flag signal of the Video chroma Cb

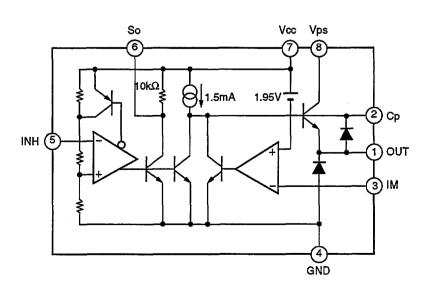
No.	Pin Name	1/0	Pin Function	No.	Pin Name	1/0	Pin Function												
41	VBLK	0	Composite blanking output and clock reference signal Selectable by mode setting	77	ANCK	0	Clock signal at ancillary data output												
42	VCBF	0	Color burst insertion position signal	78	GND	-	Ground pin												
43	VLSW	0	Line switch (at PAL used)	79	DREQ	0	Request signal when stream input via the host path.												
44	vvs	0	Vertical sync. signal output Also selectable to vertical reset signal by mode setting.	80	DACK	1	Acknowledge signal when stream input via the host path.												
45	VHS	0	Horizontal sync. signal output Selectable to composite sync. signal or horizontal reset signal by mode register setting	81	A44E	0	Status signal of sampling clock of the decode When compound with 44.1kHz, it becomes "H".												
46	GND	_	Ground pin	82	CK_AU	1	Audio sampling clock input												
	VCK	0	Video data clock output Frequency outputs to 27MHz and 13.5MHz.	83	VDD	-	Power supply pin												
48	VDD		Power supply pin	84	RESET	1	Reset input												
49	VDC0			85	нмот	I	Host interface mode selection HMOT: When set to H, it becomes bus mode of 68 system.												
50	VDC1		Video chroma Cb and Cr output	86	HIRQ	0	Interrupt request signal to the host This pin becomes active when accepting the interrupt. This pin is tri-state output.												
51	VDC2	0	0	0	0	0	0	0	0	0	0	0	0	0	These pins output Cb and Cr video signal at 16 bit mode.	87	HRDY	0	Tri-state ready output Communicate the end of bus cycle to the host CPU in the 68k mode. Use for Wait signal in the 78k0 mode.
52	VDC3			88	HWR	1	Enable signal when the host is wrote Input WR signal in the 78k bus mode. Input R/W signal in the 68k bus mode.												
53	GND	_	Ground pin	89	HRD	ı	Enable signal when the host is readed Input RD signal in the 78k bus mode. Input data strobe signal in the 68k bus mode.												
54	VDC4			90	HCS	_	Chip select signal of active "L"												
55	VDC5	0	eo chroma Cb and Cr output se pins output Cb and Cr video signal at 16	91	HALE	ı	Address latch enable signal When address and data is not multiplexed, pull- up to "H".												
56	VDC6		bit mode.		GND	_	Ground pin												
57	VDC7			93	HD0														
	VDD	_	Power supply pin		HD1	1/0	Data bus for 8 bit host interface Lower 8 bit address of the host is able to input												
	VDY0		Video data output		HD2		with multiplex.												
	VDY1		Output Y data only at 16 bit mode.	96 97	HD3														
	VDY2		Output Cb, Y, Cr and Y video format at 8 bit mode.		VDD		Power supply pin												
	VDY3				HD4		Data bus for 8 bit host interface												
	GND	_	Ground pin		HD5	1/0	Lower 8 bit address of the host is able to input												
	VDY4 VDY5		Video data output		HD6 HD7		with multiplex.												
	VDY6		Output Y data only at 16 bit mode.  Output Cb, Y, Cr and Y video format at 8 bit		GND		Ground pin												
	VDY6 VDY7		mode.		HA0		Jarouna piii												
	VDT/		Power supply pin		HA1		Host address hus input												
	ADO		PCM data output		HA2	i	Host address bus input This address bus is able to multipled to HD7-0												
	ABCK	0	Audio data clock output		HA3		•												
	ALRCK		LR switching signal		VDD		Power supply pin												
	AMCK		Master clock for audio Outputs same frequency as CK_AU pin		HA4		A STEEDY FOR												
73	AEMP2	0	Emphasis output When existing the emphasis in conformity to 50 / 15μs, outputs "H".	109	HA5	ì	Host address bus input This address bus is able to multipled to HD7-0												
	AEMP1	0	Emphasis output When existing the emphasis in conformity to ITU-TJ.71, outputs "H".		HA6		This address bus is able to fittilipled to HD7-0												
	ASTB	0	Ancillary strobe signal		HA7														
76	ADATA	0	Ancillary data output	112	GND	1	Ground pin												

No.	Pin Name	1/0	Pin Function	No.	Pin Name	ľO	Pin Function	
113	ТМо	ı	Test mode input	137	MST4			
114	TM1	•	Connect to GND excepting test.	138	MSТЗ			
115	TS0			139	MST2	0	Test output Set to open in the actual use.	
116	TS1			140	MST1			
117	TS2	0	Test output	141	MST0			
118	TS3	0	Set to open in the actual use.	142	VDD	-	Power supply pin	
119	TS4			143	MA9			
120	TS5				MA8			
121	VDD	-	Power supply pin	145	MA7	0	Address output Output low address to MA11-0 and column	
122	SDATA7			146	MA6		address to MA8-0 with multiplex.	
123	SDATA6		A/V PES stream data bus	147	MA5			
124	SDATA5	•		148	MA4			
125	SDATA4			149	GND		Ground pin	
126	GND	_	Ground pin	150	МАЗ			
127	SDATA3			151	MA2			
	SDATA2	1	AN PES stream data bus		MA1	0	Address output Output low address to MA11-0 and column	
	SDATA1	'	'	NV FLO SHEATH GAIA DUS	153	MAO		address to MA8-0 with multiplex.
	SDATA0				MA10			
	VDD	_	Power supply pin		MA11			
132	SV_STB	ı	Video PES stream data strobe signal	156	MCS	0	Chip select output	
133	SA_STB	-	Audio PES stream data strobe signal	157	MRAS	0	Low address strobe signal	
134	SV_REQ	0	Video PES stream data request signal	158	MCAS	0	Column address strobe signal	
135	SA_REQ	0	Audio PES stream data request signal	159	MWE	0	Write enable signal	
136	GND	_	Ground pin	160	VDD	_	Power supply pin	

# ■ IR3C07N (DVD MAIN ASSY : IC995)

# • LASER DIODE DRIVER

## Block Diagram



No.	Mark	Pin Function
1	OUT	Output
2	Ср	Phase compensation
3	IM	Monitor input
4	GND	Ground
5	INH	Inhibit input (ON, OFF)
6	So	Operating signal output
7	Vcc	Power supply for control circuit
8	Vps	Power supply for laser driver

# ■ UPD4516161G5-A12-7JF (DVD MAIN ASSY : IC421)

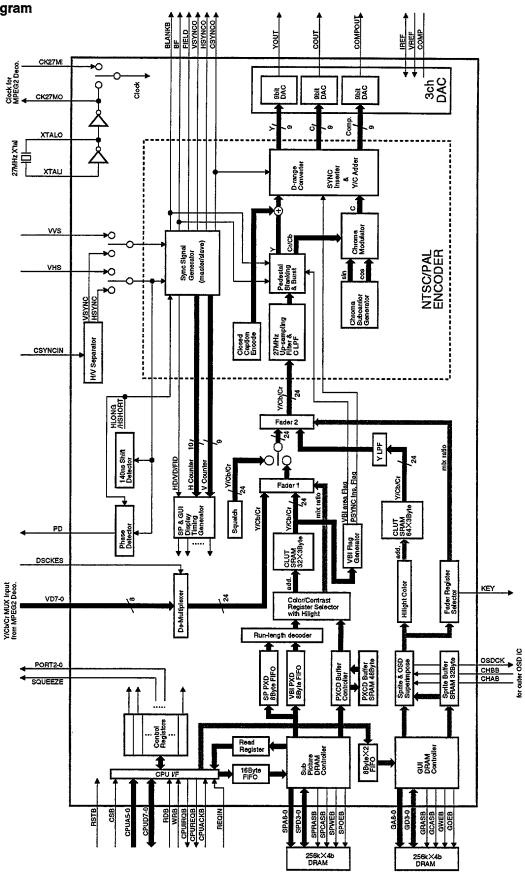
## • SYNCHRONOUS DRAM

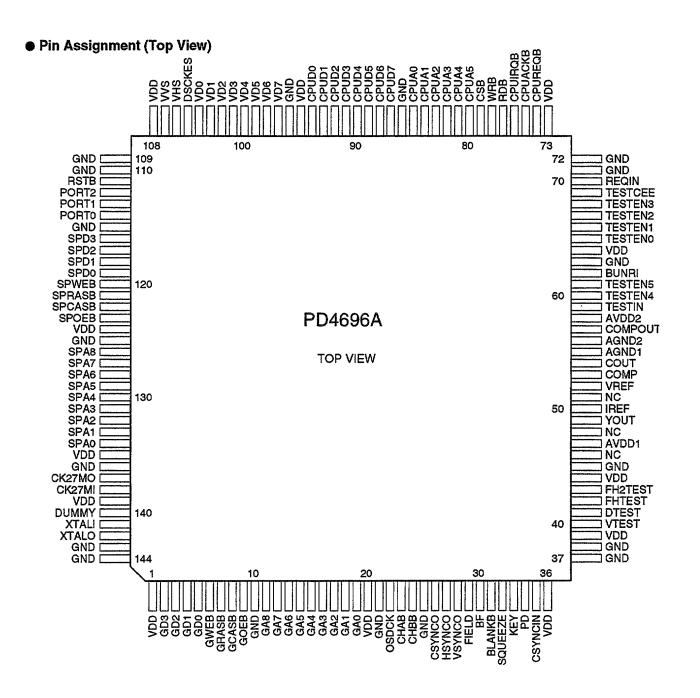
No.	Pin Name	Pin Function	No.	Pin Name	Pin Function	
1	Vcc	Power supply	26	Vss	Ground	
2	DQ0	Data innertial thresh	27	A4		
3	DQ1	Data input/output	28	A5		
4	VssQ	Ground for DQ	29	A6	Address input	
5	DQ2	Data input/output	30	A7	Address riput	
6	DQ3	Data Inpuvoutput	31	A8		
7	VccQ	Power supply for DQ	32	A9		
8	DQ4	Paka immusida sikarah	33	NC	Non connection	
9	DQ5	Data input/output	34	CKE	Clock enable	
10	VssQ	Ground for DQ	35	CLK	System clock input	
11	DQ6	Data input/output	36	UDQM	Upper DQ mask enable	
12	DQ7	Data Input/output	37	NC	Non connection	
13	VccQ	Power supply for DQ	38	VccQ	Power supply for DQ	
14	LDQM	Low DQ mask enable	39	DQ8	Data input/output	
15	WE	Write enable	40	DQ9	Data ii puvoutput	
16	CAS	Column address strobe	41	VssQ	Ground for DQ	
17	RAS	Row address strobe	42	DQ10	Data input/output	
18	cs	Chip select	43	DQ11	Data inpuroutput	
19	A11		44	VccQ	Power supply for DQ	
20	A10		45	DQ12	Data input/output	
21	A0	Address input	46	DQ13	Data inputouput	
22	A1	Address lilput	47	VssQ	Ground for DQ	
23	A2	- -		DQ14	Data input/output	
24	А3			DQ15	Data ii pas varpat	
25	Vcc	Power supply	50	Vss	Ground	

# **■ PD4696A (DVD MAIN ASSY : IC501)**

VIDEO ENCODER

Block Diagram





No.	Name	I/O	Function
1	VDD	<u> </u>	Power terminal. Connect to +3.3 V (VDD of the logic system).
2	GD3		
3	GD2	NO	DRAM data input/output for GUI. Connect to data input/output of 256 k54 bits DRAM.
4	GD1		
5	GD0		
6	GWEB	0	/WE output to DRAM for GUI. Connect to the /WE terminal of 256 k54 bits DRAM.
7	GRASB	0	/RAS output to DRAM for GUI. Connect to the /RAS terminal of 256 k54 bits DRAM.
8	GCASB	0	/CAS output to DRAM for GUI. Connect to the /CAS terminal of 256 k54 bits DRAM.
9	GOEB	0	/OE output to DRAM for GUI. Connect to the /OE terminal of 256 k54 bits DRAM.
10	GND	-	Grounding terminal. Connect to GND (GND of the logic system).

No.	Name	I/O	Function
11	GA8	+	
12	GA7	7	
13	GA6	1	
14	GA5	┨	
15	GA4	١,	Address output of DRAM for GUI. Connect to address output of 256 k54 bits DRAM.
16	GA3	⊢	GAO is LSB, and GA8 is MSB.
17	GA2	-	one is 200, and one is middle
18	GA1	┥	
19	GA0	=	
20	VDD	+-	Power terminal. Connect to +3.3 V (VDD of the logic system).
21	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
22	OSDCK	0	
23	CHAB	I	Clock output when using OSD IC as external. Connect to clock input of OSD IC (6.75 MHz).
23	CHAB	1	Connects character output of OSD IC when using the OSD IC as external. Character colors from the color pallet according to
24	СНВВ	+ -	OSD mode will be superimposed on video output when the system is set to "L".
24	Спвв	I	Connects character frame output of OSD IC when using the OSD IC as external. Character frame colors from the color pallet
105	OVD.		according to OSD mode will be superimposed on video output when the system is set to "L".
25	GND	<u>  -</u>	Grounding terminal. Connect to GND (GND of the logic system).
26	CSYNCO	0	Composite sync output from built-in SSG. Synchronizes video output (negative logic).
27	HSYNCO	0	H sync output from built-in SSG. Synchronizes video output (negative logic).
28	VSYNCO	0	V sync output from built-in SSG. Synchronizes video output (negative logic).
29	FIELD	0	Field output from built-in SSG. Synchronizes the field of video output. Indicates "Odd" when the system is set to "H" and
	. <u> </u>	$\perp$	"Even" when "L".
30	BF	0	Burst flag output from built-in SSG. The system indicates the position of burst of video output with "H".
31	BLANKB	0	Blanking output from built-in SSG. The system indicates the blanking area between H and V of video output with "L".
32	SQUEEZE	0	Outputs the content of built-in register of the same name.
33	KEY	0	Outputs "H" if the value of fader corresponding the value of pixel of GUI is other than zero (0) when the value of KEY_EN
1			register is "H" Otherwise outputs "L" Synchronizes the pixel position of video output (delay is also possible). The system is
1			fixed.
34	PD	0	Outputs the result of comparison of phases of H sync of external input and H sync of built-in SSG in three states. "L"/"H"
			shows the polarity, and the pulse width shows the phase difference. ON/OFF and polarity of output are set by the register.
35	CSYNCIN	$+_{\overline{1}}$	Composite sync input for external synchronization. The composite sync separates into H sync and V sync inside the system to
			synchronize built-in SSG or output the results of comparison of H phases from PD.
36	VDD	<del>  -  </del>	Power terminal. Connect to +3.3 V (VDD of the logic system).
37	GND	+-	Grounding terminal. Connect to GND (GND of the logic system).
38	GND	1 -	Grounding terminal. Connect to GND (GND of the logic system).
39	VDD	1 - 1	Power terminal. Connect to +3.3 V (VDD of the logic system).
40	VTEST	+-i	Tower terminal. Commercial 15.5 v (vbb of the togets system).
41	DTEST	┪.╽	Test terminal. Leave it open (terminal for IC test).
	FHTEST	-	A De Communication of the Comm
_	FH2TEST	-	
	VDD	+	Power terminal. Connect to +3.3 V (VDD of the logic system).
	GND	+ -	Grounding terminal. Connect to GND (GND of the logic system).
	NC	+-	No connection. Leave it open.
		1-1	Power terminal. Connect to +3.3 V (VDD of the logic system).
	AVDD1	┿	
	NC	ᅷ	No connection. Leave it open.
49	YOUT	0	Analog video output of luminance signal. Composite sync signal is superimposed. Connect the load of standard 150Ωbetween
	mre	1.1	GND of the analog system.
50	IREF	I	Terminal for adjustment of video output current (full-scale current). Connect the reference resistor of standard 1.1kΩ between
	11.0	1_1	GND of the analog system.
	NC	1:1	No connection. Leave it open.
	VREF	I	Terminal for adjustment of video output current (full-scale current). Apply the reference voltage of standard 1.0V.
53	COMP	I	Terminal to compensate phase of built-in DA convertor. Connect the capacitor of standard 0.1ΩF between GND of the analog
			system.
	COUT	0	Analog video output of color signal. Connect the load of standard 150 $\Omega$ between GND of the analog system.
	AGND1	<u> </u>	Grounding terminal. Connect to GND (GND of the analog system).
56	AGND2	] -	Grounding terminal. Connect to GND (GND of the analog system).
57	COMPOUT	0	Analog video output of composite video signal. Composite sync signal is superimposed. Connect the load of standard 150a+
			between GND of the analog system.
58	AVDD2	1 - 1	Power terminal. Connect to +3.3 V (VDD of the analog system).
59	TESTIN	1	
	TESTEN4	7 - I	Test terminal. Leave it open (terminal for IC test).
61	TESTEN5		
	BUNRI	┧	

## PD4696A

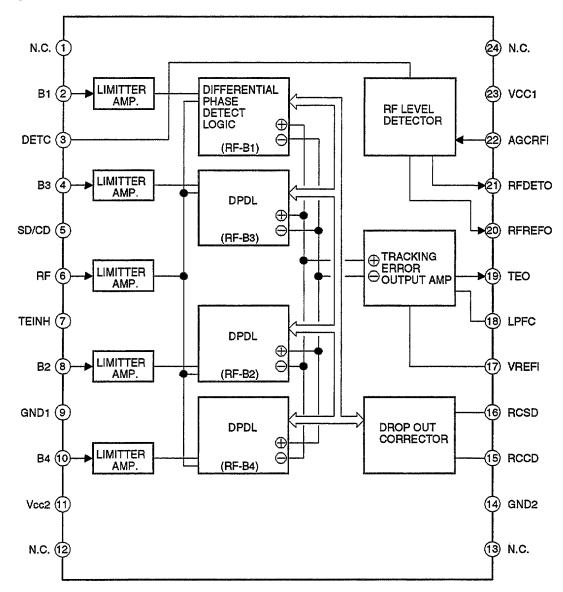
			PD4696A
No.	Name	NO	Function
63	GND	-	Grounding terminal. Connect to GND (GND of the analog system).
64	VDD	-	Power terminal. Connect to +3.3 V (VDD of the analog system).
65	TESTENO		
66	TESTEN1	1	
67	TESTEN2	1 .	Test terminal. Leave it open (terminal for IC test)
68	TESTEN3	1	
69	TESTCCE	-	
	REQIN	$+_{\rm I}$	Inputs request signal of the DMA source if OR logic is required for transfer enable request of the external IC (DMA source)
′	KEQII1	*	and DMA request of this IC.
71	GND	+	Grounding terminal. Connect to GND (GND of the analog system).
72	GND	1-1	Grounding terminal. Connect to GND (GND of the analog system).
73	VDD	1	Power terminal. Connect to +3.3 V (VDD of the analog system).
74	CPUREQB	0	DMA request signal. Connect to DMA request input of CPU IC. The DMA request is roughly classified into the request for
			subvideo data and the request for GUI data. Either requests are executed by the instruction of the DMA start command to
1 1			the corresponding register. The "L" level of the DMA request signal indicates that the request is being made. The system
		1 1	automatically sets to "H" if built-in FIFO becomes full or transmission of the required amount of data is completed. THe
			DMA request signal can use OR logic with REQIN input.
75	CPUACKB	I	Connect acknowledge output from CPU IC during DMA request. The system retrieves data input to CPUD7-0 into biult-in
			FIFO at the leading edge of this signal.
76	CPUIRQB	0	Interrupt signal to CPU IC. Connect to interrupt input of CPU IC. The system generates "L" signal every time the V
	-		blanking of video output is encountered.
77	RDB	I	Read signal when the CPU IC wants to read the content of the read register. The content of the register of the address being
			accessed will be output to CPU7-0 when the system is set to "L".
78	WRB	$+_{\bar{1}}$	Write signal when the CPU IC wants to rewrite the content of the read register. Connects write output of CPU IC. The
~	··· ita	^	content of the register of the address being accessed will be rewritten to the data being input to CPU7-0 when the system is
			set to "L".
79	CSB	$+_{\overline{1}}$	Selection signal when the CPU IC wants to read or write the register of this IC. Connects CS output of CPU IC.
80	CPUA5	<u> </u>	Selection signal when the CFO IC wants to read of write the register of this IC. Connects CS output of CFO IC.
		-	
	CPUA4	-1 , 1	All College of the Co
82	CPUA3	I	Address signal when the CPU IC wants to read or write the register of this IC.
83	CPUA2	-	Connects address output of CPU IC. CPUA0 is LSB, and CPUA5 is MSB.
84	CPUAI	4	
85	CPUAO		
86	GND		Grounding terminal. Connect to GND (GND of the logic system).
87	CPUD7	]	
88	CPUD6		
89	CPUD5	J	
90	CPUD4	Ю	Data signal when the CPU IC wants to read or write the register of this IC, and transmission data signal during DMA
			transmission.
91	CPUD3		Connects to data bus under the CPU IC. CPUD0 is LSB, and CPUD7 is MSB.
92	CPUD2	1	
93	CPUD1	1	
94	CPUD0	7 I	
	VDD	1-1	Power terminal. Connect to +3.3 V (VDD of the logic system).
96	GND	<b>†</b> -	Grounding terminal. Connect to GND (GND of the logic system).
97	VD7	+	
98	VD6	1	
99	VD5	1	
100	VD4	- I	Connects video data signal output of 8-bit multiplex mode of the MPEG2 decoder IC. VD0 is LSB, and VD7 is MSB.
	VD3	┨	COMMEND . THE CHAIR CONTROL OF C OF THE METERS OF CO. OF THE THE THE TANK OF THE CO. OF THE TANK OF TH
	VD2	-	
	VD1	-	
		-{	
	VD0	┤┯┤	Signal to select whether retrieve video data signal input from VD7-0 at the leading edge or trailing edge of the internal 27
100	DSCKES	I	
اليا	*****	1	MHz clock. The system selects the leading edge at "L" or open, and selects the trailing edge at "H".
106	VHS	Ι	Connects H sync output from the MPEG2 decoder. Must be synchronized with VD7-0 (negative logic). Synchronizes built-
لـــا			in SSG, and outputs the result of comparison of H phases from PD.
107	VVS	I	Connects V sync output from the MPEG2 decoder. Must be synchronized with VD7-0 (negative logic). Synchronizes built-
			in SSG.
	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
109	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
	GND	-	Grounding terminal. Connect to GND (GND of the logic system).

No.	Name	ľO	Function				
111	RSTB	I	Reset input for IC as a whole. The built-in register, circuitry, etc. will be initialized when the system is set to "L".				
112	PORT2						
113	PORT1	0	Outputs the content of the built-in register of the same name.				
114	PORT0	1					
115	GND	-	Grounding terminal. Connect to GND (GND of the logic system).				
116	SPD3						
117	SPD2	10	Data input/output of DRAM for subvideo. Connect to data input/output of 256 kü~4 bits DRAM.				
118	SPD1	1 1	namingas cupas of Dictaria sucritation Conflows to and impurousput of 200 na 7 orb Dictaria.				
119	SPD0	1					
120	SPWEB	0	/WE output to DRAM for subvideo. Connect to the /WE terminal of 256 k54 bits DRAM.				
121	SPRASB	0	/RAS output to DRAM for subvideo. Connect to the /RAS terminal of 256 k54 bits DRAM.				
122	SPCASB	0	/CAS output to DRAM for subvideo. Connect to the /CAS terminal of 256 k54 bits DRAM.				
123	SPOEB	0	/OE output to DRAM for subvideo. Connect to the /OE terminal of 256 k54 bits DRAM.				
124	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).				
125	GND	-	Grounding terminal. Connect to GND (GND of the logic system).				
126	SPA8						
127	SPA7	]					
128	SPA6	]					
129	SPA5						
130	SPA4	0	Address output of DRAM for subvideo. Connect to address output of 256 k54 bits DRAM. SPA0 is LSB, and SPA8 is MSB.				
131	SPA3	1					
132	SPA2	1					
133	SPA1	1					
134	SPA0	1 '					
-	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).				
	GND	-	Grounding terminal. Connect to GND (GND of the logic system).				
		0	27 MHz clock output from built-in X'tal OSC. The terminal is buffered, and can drive external circuit.				
138	CK27MI	I	27 MHz system clock input during external input mode of this IC. Inputs rectangular wave of 27 MHz.				
139	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).				
140	DUMMY	0	Dummy output of built-in X'tal OSC. Normally leave it open.				
141	XTALI	I	Input of built-in X'tal OSC. Use the terminal by connecting the X'tal to external circuit.				
142	XTALO	0	Output of built-in X'tal OSC. Use the terminal by connecting the X'tal to external. Cannot supply the clock to external				
			circuit from this terminal. Should use CK27MO. For the system clock of this IC, this signal is internally buffered during internal input.				
143	GND	-	Grounding terminal. Connect to GND (GND of the logic system).				
	GND		Grounding terminal. Connect to GND (GND of the logic system).				

## ■ PA0065AM (DVD MAIN ASSY: IC601)

• TIME-DIFFERENCE IC

## Block Diagram

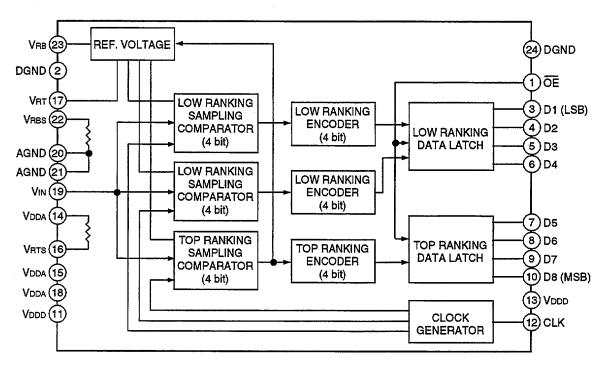


No.	Pin Name	Pin Function	No.	Pin Name	Pin Function
1	NC	Non connection	13	NC	Non connection
2	B1	B1 signal input	14	GND2	Ground
3	DETC	Connect a capacitor for RF level detection	15	RCCD	Time constant for limit the pulse width of CD mode
4	B3	B3 signal input	16	RCDVD	Time constant for limit the pulse width of DVD mode
5	DVD/CD	DVD/CD mode switching signal input H : DVD mode, L : CD mode	17	VREFI	Reference voltage input
6	RF	RF signal input	18	LPFC	Low pass filter for TE output
7	TEINH	TE output prohibition signal input	19	TEO	TE output
8	B2	B2 signal input	20	RFREFO	Reference voltage output for RF level detection
9	GND1	Ground	21	RFDETO	RF level detecting output
10	B4	B4 signal input	22	AGCRFI	AGCRF signal input
11	VCC2	5V power supply	23	VCC1	5V power supply
12	NC	Non connection	24	NC	Non connection

## ■ TLC5540INS (DVD MAIN ASSY: IC731)

## ● A/D CONVERTER

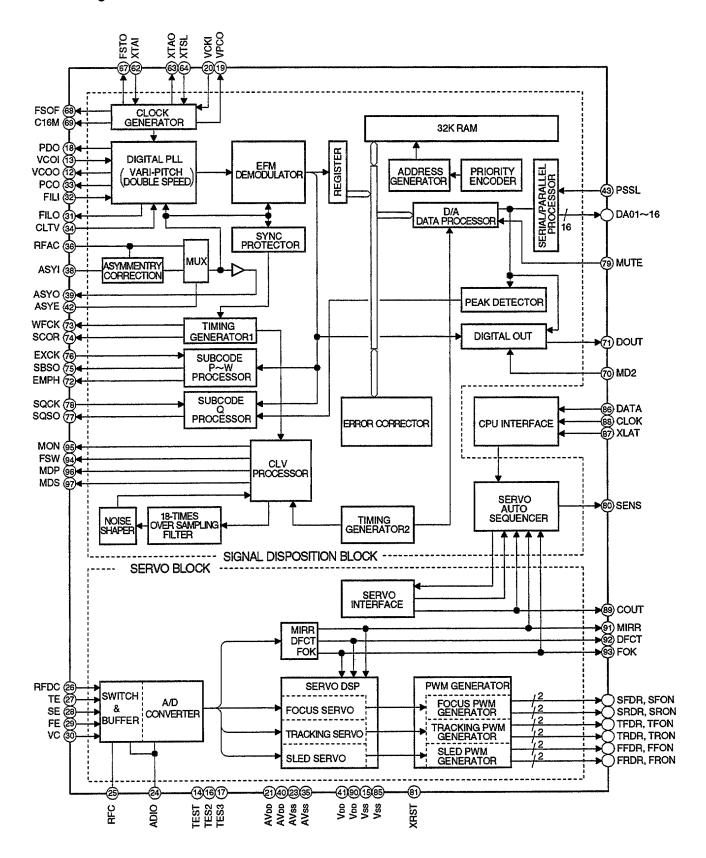
## Block Diagram



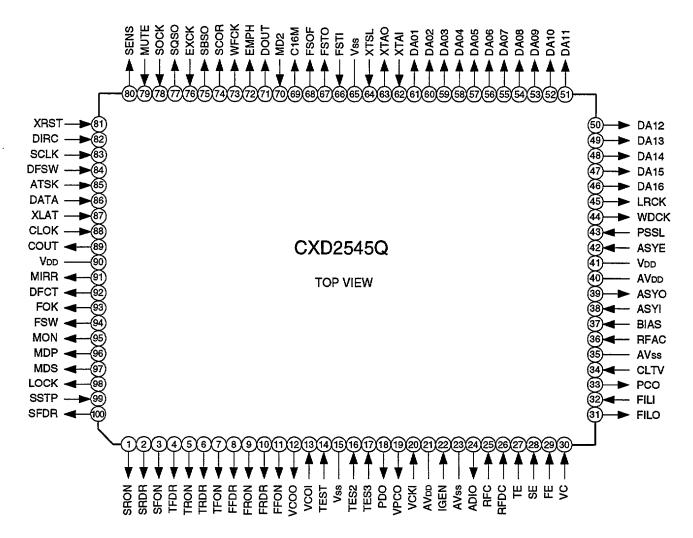
No.	Pin Name	1/0	Pin Function
1	ŌE	ı	Output enable OE="L" level : Data enable OE="H" level : Output high impedance
2, 24	DGND	_	Ground for Digital system
3-10	D1-D8	0	Digital output D1: LSB, D8 : MSB
11, 13	VDDD	_	Power supply for Digital system
12	CLK	ı	Clock input
16	VRTS	_	Reference voltage output (upper) Short-circuit to VRT in the internal reference voltage used. Generates a 2.63V.
17	VRT	ī	Reference voltage output (upper)
23	VRB	ı	Reference voltage output (lower)
14, 15, 18	VDDA	_	Power supply for Analog system
19	Vin	1	Analog input
20, 21	AGND	_	Ground for Analog system
22	VRBS	_	Reference voltage output (upper) Short-circuit to VRT in the internal reference voltage used. Generates a 0.61V.

## CXD2545Q (DVD MAIN ASSY : IC801)

- DIGITAL SERVO IC
- Block Diagram



## Pin Assignment (Top View)



No.	Name	I/O	Function
1	SRON	0	,
2	SRDR	0	Thread drive output.
3	SFON	0	
4	TFDR	0	
5	TRON	0	
6	TRDR	0	Tracking drive output.
7	TFON	0	
8	FFDR	0	
9	FRON	0	
10	FRDR	0	Focus drive output.
11	FFON	0	
12	VCOO	0	Oscillation circuit output for analog EFM PLL.
13	VCOI	I	Oscillation circuit input for analog EFM PLL. flock = 8.6436MHz.
14	TEST	I	TEST terminal, Normally GND.
15	Vss	-	Digital GND.
16	TES2	I	TEST terminal. Normally GND.
17	TES3	I	TEST terminal. Normally GND.
18	PDO	0	Charge-pump output for analog EFM PLL.
19	VPCO	0	PLL charge-pump output for variable pitch.
20	VCKI	I	Clock input from external VCO for variable pitch.fcenter = 16.9344MHz.

No.	Name	ľO	Function
21	AVDD	-	Analog power supply.
22	IGEN	I	Terminal to connect the current source reference resistor of the operational amplifier for digital servo.
23	AVss	-	Analog GND.
24	ADIO	0	A/D converter input monitor terminal.
25	RFC	I	Terminal to connect the low-pass filter capacitor for RFDC input.
26	RFDC	I	RF signal input. Input range: 2.15 to 5.0 V (when VDD = AVDD = 5.0 V).
27	TE	I	Tracking error signal input. Input range: 2.5~1.0 V (when VDD = AVDD = 5.0 V).
28	SE	I	Thread-error signal input. Input range: 2.5~1.0 V (when VDD = AVDD = 5.0 V).
29	FE	I	Focus-error signal input. Input range: 2.5-1.0 V (when VDD = AVDD = 5.0 V).
30	VC	I	Mid-point voltage input terminal.
31	FILO	0	Filter output for master PLL.
32	FILI	0	Filter input for master PLL.
33	PCO	0	Charge-pump output for master PLL.
34	CLTV	I	VCO control voltage input for master.
35	AVss	-	Analog GND.
36	RFAC	I	EFM signal input.
37	BIAS	I	Asymmetrical circuit constant current input.
38	ASYI	I	Asymmetrical comparison voltage input.
39	ASYO	0	EFM full-swing output ( $L = Vss$ , $H = Vdd$ ).
40	AVDD	-	Analog power supply.
41	V <sub>DD</sub>	-	Digital power supply.
42	ASYE	I	Asymmetrical circuit ON/OFF ( L = OFF, H = ON).
43	PSSL	I	Audio data output mode switching input (L = serial output, H = parallel output).
44	WDCK	0	48-bit slot D/A interface. Word clock (f = 2 Fs).
45	LRCK	0	48-bit slot D/A interface. OR clock (f = Fs).
46	DA16	0	DA16 output when PSSL = 1. Serial data of 48-bit slot when PSSL = 0.
47	DA15	0	DA15 output when PSSL = 1. Bit clock of 48-bit slot when PSSL = 0.
48	DA14	0	DA14 output when PSSL = 1. Serial data of 64-bit slot when PSSL = 0.
49	DA13	0	DA13 output when PSSL = 1. Bit clock of 64-bit slot when PSSL = 0.
50	DA12	0	DA12 output when PSSL = 1. LR clock of 64-bit slot when PSSL = 0.
51	DA11	0	DA11 output when PSSL = 1. GTOP output when PSSL = 0.
52	DA10	0	DA10 output when PSSL = 1. XUGF output when PSSL = 0.
53	DA09	0	DA09 output when PSSL = 1. XPLCK output when PSSL = 0.
54	DA08	0	DA08 output when PSSL = 1. GFS output when PSSL = 0.
55	DA07	0	DA07 output when PSSL = 1. RFCK output when PSSL = 0.
56	DA06	0	DA06 output when PSSL = 1. C2PO output when PSSL = 0.
57	DA05	0	DA05 output when PSSL = 1. XRAOF output when PSSL = 0.
58	DA04	0	DA04 output when PSSL = 1. MNT3 output when PSSL = 0.
	DA03	0	DA03~ output when PSSL = 1. MNT2 output when PSSL = 0.
60	DA02	0	DA02 output when PSSL = 1. MNT1 output when PSSL = 0.
61	DA01	0	DA01 output when PSSL = 1. MNT0 output when PSSL = 0.
62	XTAI	1	X'tal oscillation circuit input. 16.9344 MHz or 33.8688 MHz input.
63	XTAO	0	X'tal oscillation circuit output.
64	XTSL	I	X'tal selective input terminal. The system is set to L when X+tal is 16,9344 MHz, and H when 33,8688 MHz (during
			normal playback).
65	Vss	-	Digital GND.
66	FSTI	I	Reference clock input terminal for digital servo block.
67	FSTO	0	2/3 divided output for Terminals 62 and 63. Variable pitch does not change the output.
68	FSOF	0	1/4 divided output for Terminals 62 and 63. Variable pitch does not change the output.
69	C16M	0	16,9344 MHz output. Changes simultaneously with variable pitch (during normal playback).
70	MD2	I	Digital-Out ON/OFF control terminal (L = OFF, H = ON).
	DOUT	0	Digital-Out output terminal.
	EMPH	0	Emphasis mode output of the disc played back (L = no emphasis, H = emphasis).
73	WFCK	0	WFCK output.
74	SCOR	0	Subcode sync output terminal (The system sets to H when either subcode sync S0 or S1 is detected.).
75	SBSO	0	Serial output of Sub-P to Sub W.

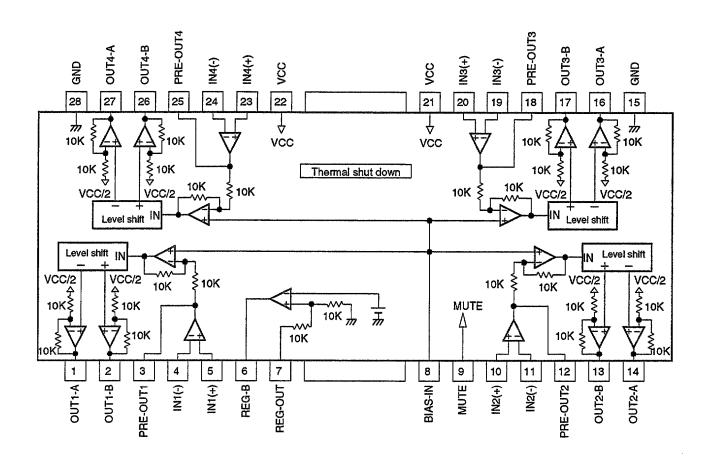
No.	Name	I/O	Function
76	EXCK	I	Clock input for SBSO read out.
77	SQSO	0	Sub-Q 80-bit output, PCM peak data, level data 16-bit output.
78	SQCK	I	Clock input for SBSO read out.
79	MUTE	I	Mute switching terminal (H = Mute).
80	SENS	0	SENS output. Outputs to CPU.
81	XRST	I	System reset ( $L = reset$ ).
82	DIRC	I	Used when skipping a single track. (Inputs VDD level when not used.)
83	SCLK	I	Clock for reading SENS serial data.
84	DFSW	I	DFCT switching terminal (H = DFCT measure circuit OFF).
85	ATSK	I	Antishock terminal.
86	DATA	I	Inputs serial data from the CPU.
87	XLAT	I	Inputs latch from the CPU.
88	CLOK	I	Inputs serial data transfer clock from the CPU.
89	COUT	0	Track counting signal output.
90	VDD	-	Digital power supply.
91	MIRR	0	Mirror signal output.
92	DFCT	0	Defect signal output.
93	FOK	0	Focus OK output.
94	FSW	0	Outputs switching the output filter of the spindle motor.
95	MON	0	ON/OFF control output for the spindle motor.
96	MDP	0	Servo control of the spindle motor.
97	MDS	0	Servo control of the spindle motor.
98	LOCK	0	Samples GFS at 460 Hz and outputs H when GFS is H. Outputs L if GFS is L eight times continuously.
99	SSTP	I	Terminal for the signal to detect the most inner circumference of the disc.
100	SFDR	0	Thread drive output.

#### Notes:

- The 64-bit slot is 2's complementary output of LSB first. The 48-bit slot is 2's complementary output of MSB first.
- GTOP is to monitor protection of Frame sync (H: sync protective window open).
- XUGF is Frame sync obtained from EFM signal, and is negative pulse. It is signal before sync protection. "
- For XPLCK, PLL is produced so that the reverse and trailing edge of the clock of EFM PLL meet the point of change of EFM signal.
- GFS signal is set to H when Frame sync meets the interpolated protection timing.
- $\bullet$  RFCK is obtained with X'tal precision. It is signal of cycles at 136 $\pm$ s.
- C2PO is signal to express error status of data.
- XRAOF is signal generated when 32K RAM exceeds the jitter margin ofü}28 frames.

## ■ BA6797FP (DVD MAIN ASSY: IC851)

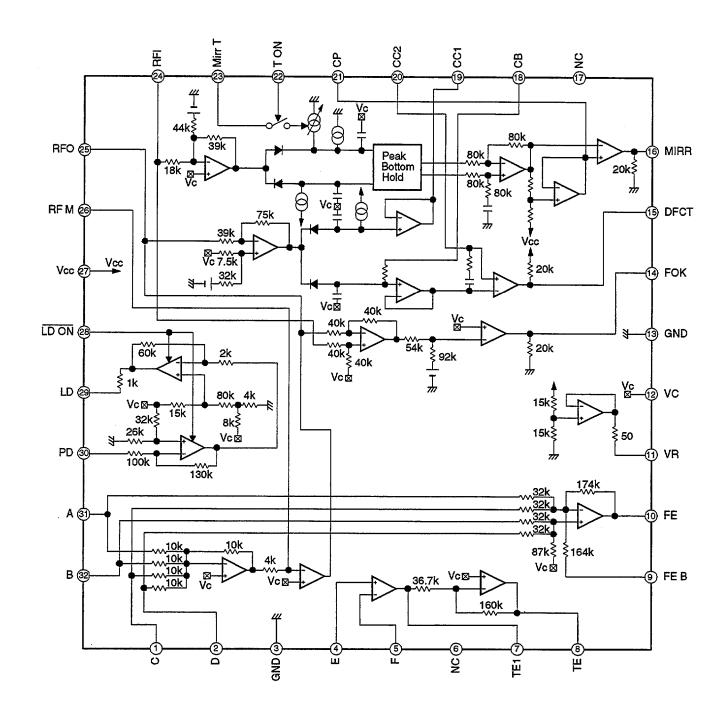
- BTL DRIVER
- Block Diagram



No.	Name	Function
1	OUT1-A	Driver CH1 output terminal.
2	OUT1-B	Driver CH1 output terminal.
3	PRE-OUT1	CH1 previous-stage amplifier output terminal.
4	IN1 (-)	CH1 previous-stage amplifier reverse input terminal.
5	IN1 (+)	CH1 previous-stage amplifier non-reverse input terminal.
6	REG-B	External Tr base connection terminal.
7	REG-OUT	Constant-voltage output (external Tr collector connection).
8	BIAS-IN	Bias input terminal.
9	MUTE	Mute control terminal.
10	IN2 (+)	CH2 previous-stage amplifier non-reverse input terminal.
11	IN2 (-)	CH2 previous-stage amplifier reverse input terminal.
12	PRE-OUT2	CH2 Previous-stage amplifier output terminal.
13	OUT2-B	Driver CH2 output terminal.
14	OUT2-A	Driver CH2 output terminal.

No.	Name	Function
15	GND	Substraight GND.
16	OUT3-A	Driver CH3 output terminal.
17	OUT3-B	Driver CH3 output terminal.
18	PRE-OUT3	CH3 previous-stage amplifier output terminal.
19	IN3 (-)	CH3 previous-stage amplifier reverse input terminal.
20	IN3 (+)	CH3 previous-stage amplifier non-reverse input terminal.
21	VCC	VCC
22	VCC	VCC
23	IN4 (+)	CH4 previous-stage amplifier non-reverse input terminal.
24	IN4 (-)	CH4 previous-stage amplifier reverse input terminal.
25	PRE-OUT4	CH4 previous-stage amplifier output terminal.
26	OUT4-B	Driver CH4 output terminal.
27	OUT4-A	Driver CH4 output terminal.
28	GND	Substraight GND.

- CXA2521AQ (DVD MAIN ASSY: IC901)
  - RF AMP
- Block Diagram

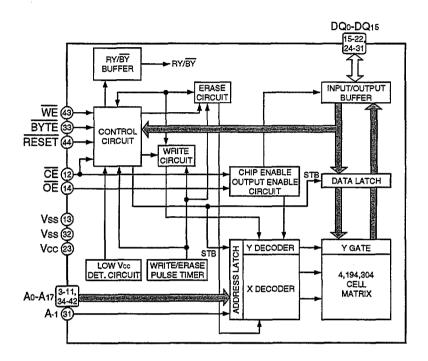


# **DVL-90, DVL-700**

No.	Name	I/O	Function
1	С	I	Input terminal for the RF summing amplifier and focus error amplifier.
2	D	I	Input terminal for the RF summing amplifier and focus error amplifier.
3	GND	-	Grounding terminal.
4	Е	I	Input terminal for the tracking error amplifier.
5	F	I	Input terminal for the tracking error amplifier.
6	NC	-	Open on the circuit.
7	TE1	0	Output for the tracking error amplifier and input terminal for the tracking error drive.
8	TE	0	Output terminal for the tracking error amplifier.
9	FE B	I	Focus bias adjusting terminal for the focus amplifier.
10	FE	0	Output terminal for the focus error amplifier.
11	VR	0	DC voltage output terminal for (Vcc + GND)/2.
12	VC	I	Mid-point voltage input terminal for VC.
13	GND	-	Grounding terminal.
14	FOK	0	Output terminal for the FOK comparator.
15	DFCT	0	Output terminal for the DEFECT comparator.
16	Mirr	0	Output terminal for the mirror comparator.
17	NC	-	Open on the circuit.
18	СВ	I	Connection terminal for the DEFECT Bottom Hold capacitor.
19	CC1	0	Output terminal for DEFECT Bottom Hold.
20	CC2	I	Input terminal to which combined capacity of output from DEFECT Bottom Hold is input.
21	СР	I	Connection terminal for the Mirror Hold capacitor and non-reverse input terminal for the mirror comparator.
22	TON	I	Time constant switching terminal for Peak Hold. Connecting the terminal to Vcc enables adjustment of time constant.
			Connecting the terminal to GND fixes time constant.
23	Mirr	I	Time constant adjusting terminal for Peak Hold. Time constant is set to that adjusted when Terminal 22 was turned to ON.
24	RFI	I	Input terminal to which combined capacity of output from the RF summing amplifier is input.
25	RFO	0	Output terminal for RF signal. The value of resistor connected between Terminals 25 and 26 determines the low-
			frequency gain of the RF drive amplifier.
26	RF M	I	Input terminal on the reverse side for the RF drive amplifier.
27	Vcc	-	Vcc pin.
28	LD ON	I	APC amplifier ON/OFF switching terminal. Connecting the terminal to Vcc turns the amplifier to OFF. Connecting the
			terminal to GNC turns the amplifier to ON.
29	LD	0	Output terminal for the APC amplifier.
30	PD	I	Input terminal for the APC amplifier.
31	A	I	Input terminal for the RF summing amplifier and focus error amplifier.
32	В	I	Input terminal for the RF summing amplifier and focus error amplifier.

# ■ MBM29F400TA-70PF (VYW1515) (DVD MAIN ASSY: IC1030)

- 4M bit FLASH MEMORY
- Block Diagram

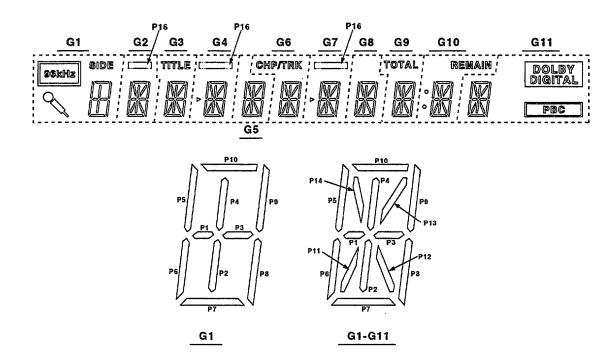


No.	Pin Name	Pin Function	No.	Pin Name	Pin Function
1	N.C.	Non connection	23	Vcc	Power supply (+5.0V ± 10% or ± 5%)
2	RY/BY	Ready/Buzy output	24	DQ4	
3	A17		25	DQ <sub>12</sub>	
4	A7		26	DQ5	
5	<b>A</b> 6		27	DQ13	Data input/output
6	<b>A</b> 5		28	DQ <sub>6</sub>	
7	A4	Address input	29	DQ14	
8	Аз		30	DQ7	
9	A2		31	DQ15/A-1	Data input / output / address input
10	A1		32	Vss	Ground
11	Ao		33	BYTE	Mode select of 8 bit and 16 bit
12	CE	Chip enable	34	A16	
13	Vss	Ground	35	A15	
14	ŌĒ	Output enable	36	A14	
15	DQ <sub>0</sub>		37	A13	
16	DQ8		38	A12	Address input
17	DQ1		39	A11	
18	DQ9	Data input /output	40	<b>A</b> 10	
19	DQ2	Data input /output	41	<b>A</b> 9	
20	DQ10		42	As	
21	DQ3		43	WE	Write enable
22	DQ11		44	RESET	Hard ware reset

## 7.1.2 DISPLAY

# **WAW1042 (FLPB ASSY: V101)**

## • FL DISPLAY



## • ANODE AND GRID ASSIGNMENT

	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11
P1	P1	P1	P1	P1	P1	P1	P1	P1	P1	P1	P1
P2	P2	P2	P2	P2	P2	P2	P2	P2	P2	P2	P2
P3	P3	Р3	Р3	P3	P3	P3	P3	Р3	P3	РЗ	P3
P4	P4	P4	P4	P4	P4	P4	P4	P4	P4	P4	P4
P5	P5	<b>P</b> 5	P5	P5	P5	P5	P5	P5	P5	P5	P5
P6	P6	P6	P6	P6	P6	P6	P6	P6	P6	P6	P6
P7	P7	P7	P7	P7	P7	P7	P7	P7	P7	P7	P7
P8	P8	P8	P8	P8	P8	P8	P8	P8	P8	P8	Pg
P9	P9	P9	P9	P9	P9	P9	P9	P9	P9	P9	P9
P10	P10	P10	P10	P10	-P10	P10	P10	P10	P10	P10	P10
P11		P11	P11	P11	P11	P11	P11	P11	P11	P11	P11
P12	8	P12	P12	P12	P12	P12	P12	P12	P12	P12	P12
P13	96kHz	P13	P13	P13	P13	P13	P13	P13	P13	P13	P13
P14		P14	P14	P14	P14	P14	P14	P14	P14	P14	P14
P15				Δ			$\geq$			0	PBC
P16	SIDE	P16	TITLE	P16		CHP/TRK	P16		TOTAL	REMAIN	BOLBY

## • PIN ASSIGNMENT

Pin No.	1	2	3	4 5	6	7	8	9	10	11.	24	25	26	27	28	29	30	31	32
Assignment	F1	F1	NP	NL P1	6 P15	P14	P13	P12	P11	N	IL	P10	P9	P8	P7	P6	NL	P5	P4
Pin No.	33	34	35	36-40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55
Assignment	РЗ	P2	P1	NL	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	NL	NP	F2	F2

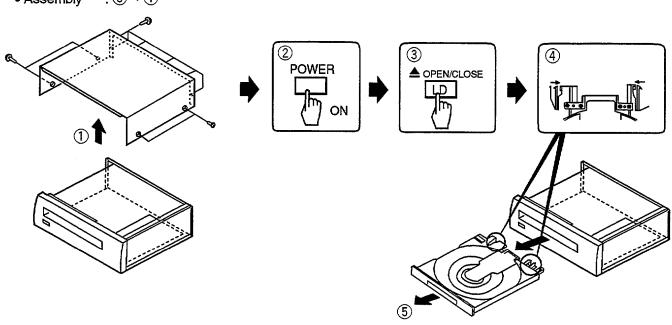
F1, F2: Filament G1-G11: Grid P1-P16: Anode NP: No Pin NL: No Lead

# 7.2 DISASSEMBLY/ASSEMBLY (分解/組立の手順)

## (1) DISC TRAY

• Disassembly :  $1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5$ 

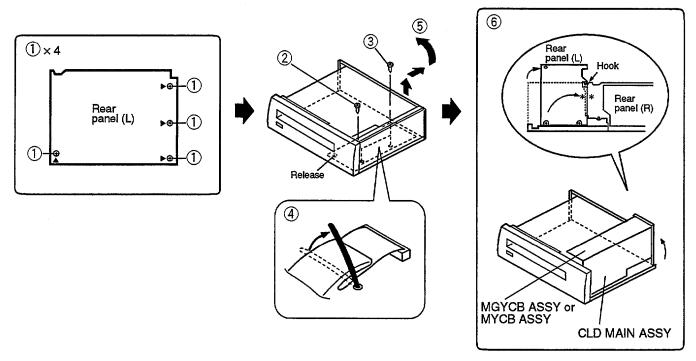
• Assembly : ⑤→①



## (2) CLD MAIN ASSY

• Disassembly : ①→②→③→④→⑤→⑥

• Assembly  $: 6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1$ 

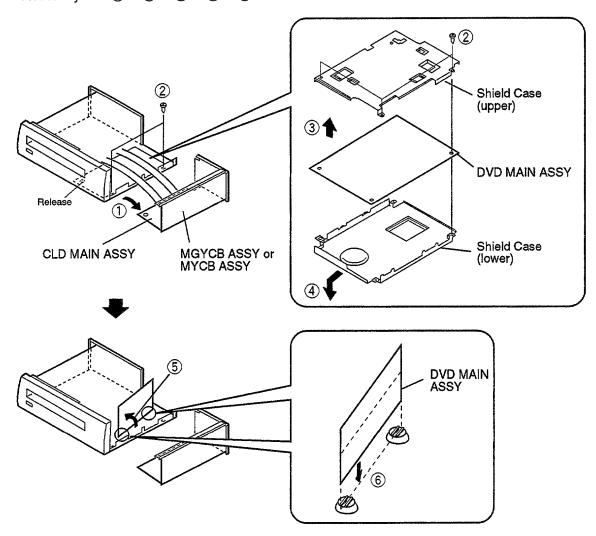


# **DVL-90, DVL-700**

# (3) DVD MAIN ASSY

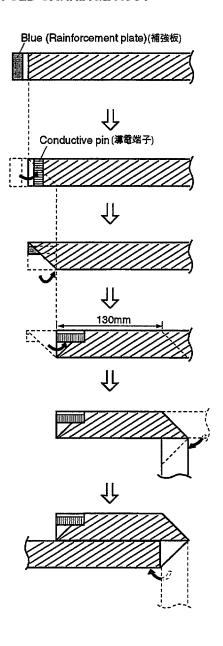
• Disassembly : ①→②→③→④→⑤→⑥

• Assembly : 6→4→3→2→1

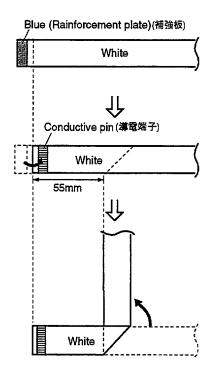


# 7.3 HOW TO BEND THE FLEXIBLE CABLE (フレキシブルケーブルの折り方)

## (1) THE FLEXIBLE CABLE FOR CLD CARRIAGE ASSY

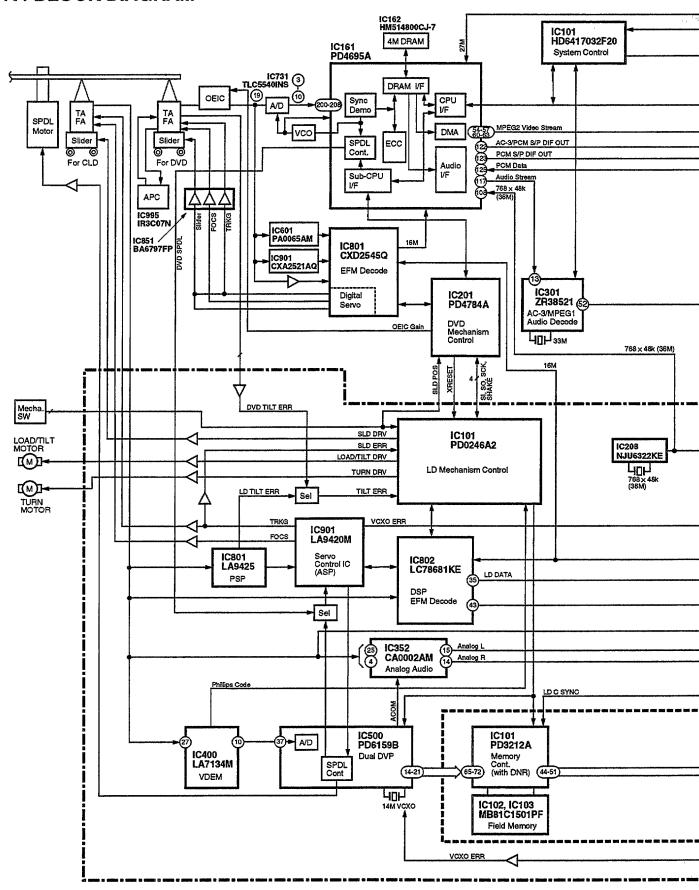


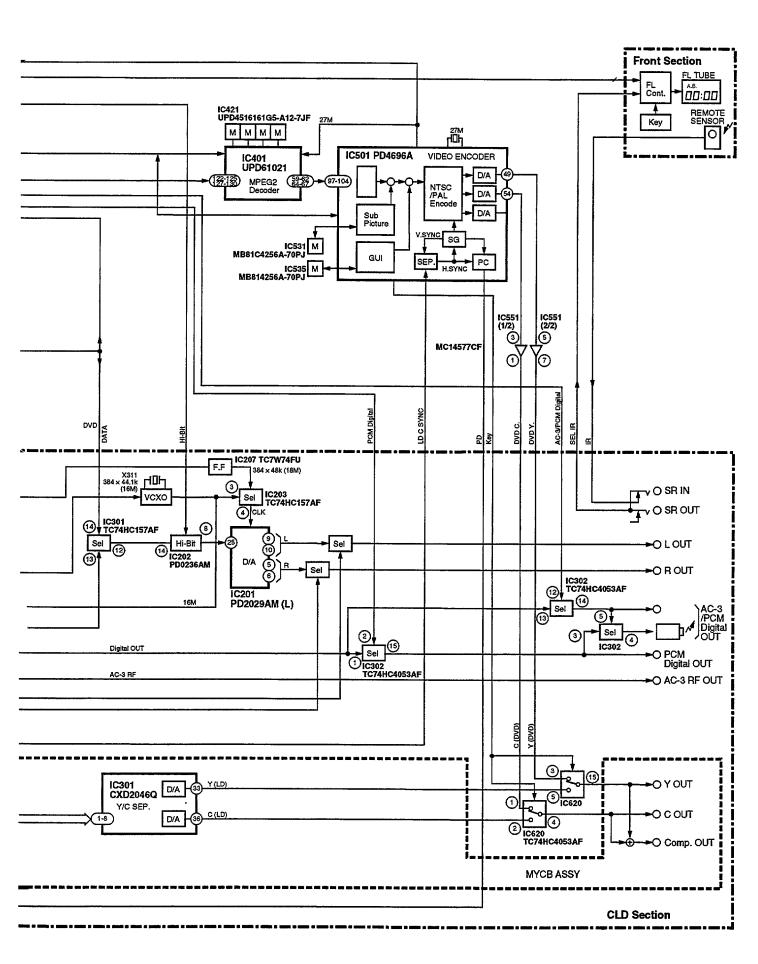
# (2) THE FLEXIBLE CABLE FOR DVD CARRIAGE ASSY



Part rating indication side (部品定格表示側)

## 7.4 BLOCK DIAGRAM

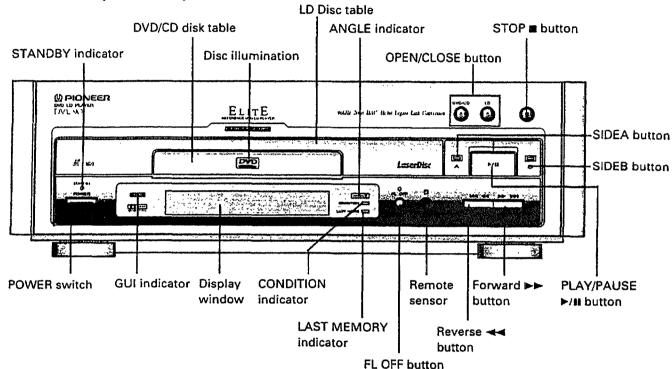


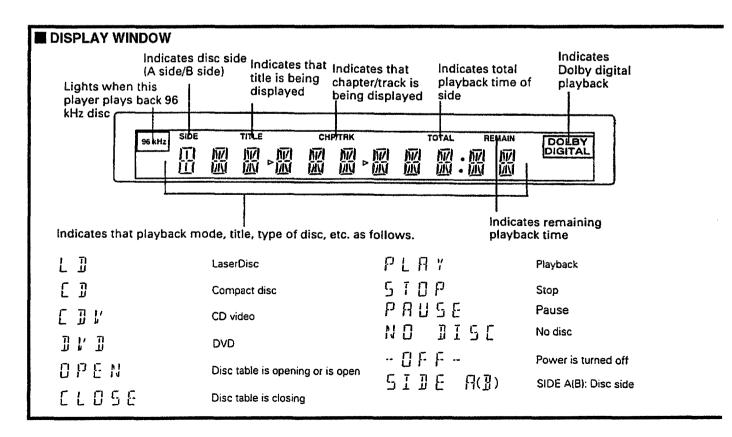


# 8. PANEL FACILITIES AND SPECIFICATIONS

#### PANEL FACILITIES







## REAR PANEL (DVL-90)

S-video output jack
1: S jack (regular S output)
2: S2 jack (simultaneously outputs recognition signal for wide TV)
S2 function is only available during DVD playback.
By connecting to the S2 jack of your wide TV etc., TV settings etc., will be switched automatically.

\* There is both 1 and 2, allowing 2 systems to be connected at the same time. For example, 1 can be connected to the TV and 2 can be connected to an AV amplifier.

		Coaxial	Connect to PCM jack
Your home	Regular AV amplifier	Optical	Connect to optical output and select PCM jack using the menu
amplifier			Connect to PCM/AC-3 jack
	AC-3 compatible amplifier	Optical	Connect optical output and select PCM/AC-3
			jack using the menu

Optical digital output jack Outputs audio as optical digital output. Can be Video output jack Audio output jack switched between AC-3/PCM and PCM 0 ⊕1 Θ **®** ➌ Control output jack Control input jack AC-3RF output (for Power cord connection terminal Digital output jack (coaxial)

By connecting to the AC-3RF jack of a receiver or processor, 5.1 ch surround audio can be enjoyed.

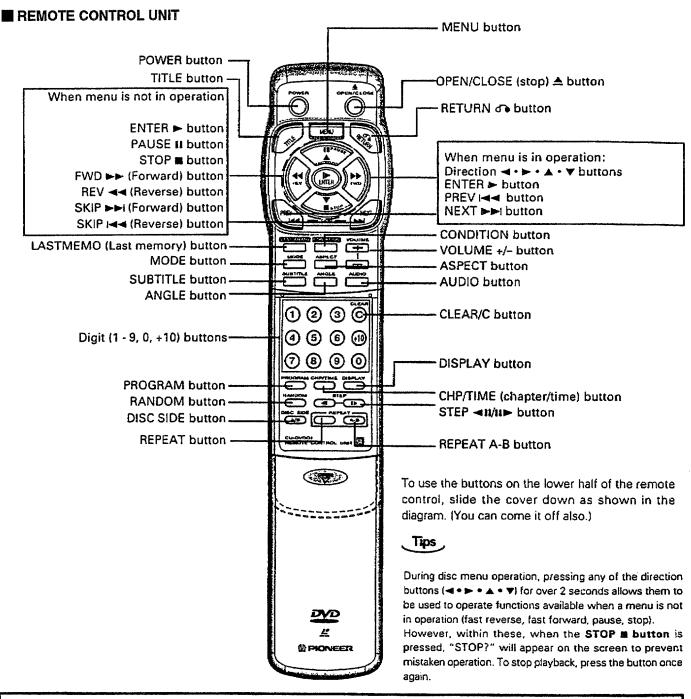
Outputs digital audio of CD, video CD and LDs with digital sound as digital output.

Depending on the other components the player is combined with, noise may be generated from the digital output jack.

When connecting to an AC-3 compatible component, please connect to the PCM/AC-3 jack.

Other components should be connected to the PCM jack. (Refer to the list above.)

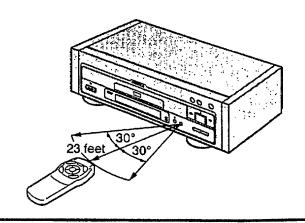
RIM	Random playback	STERED	Stereo
PROGRAM	Program mode	MENU	Menu mode
R - T R K	Repeat mode	TITLE	Title menu
R - A	Start point of 2 point repeat playback	CHRPIER	Chapter menu
R - A 3	2 point repeat playback	508-1116	Sub-title menu
R - I I L	Repeat playback of the title	SETUP	Set-up menu
R - 5 I D	Both sides of LD repeat playback	ANGLE	Angle menu
COND.MEMOR		AU 10	Audio menu
	Condition memory	DOLDY DIGIT	AL 5, 16H
LAST MEMO	Last memory playback		Dolby digital surround
CINEMAI	Cinema 1	PEM 98K	5.1 ch 96KPCM audio
CINEMAZ	Cinema 2	PEM 48K	48KPCM audio
RNIMATION	Animation mode	MPEG RUDIO	MPEG1 or MPEG2 audio
STANDARD	Standard		



# Remote control operation

When operating the remote control, point it at the remote sensor located on the player's front panel. The remote control can be used up to 23 feet (7m) from the player and within a 30" angle each side of the sensor.

- Exposing the remote sensor to direct sunlight or strong light may cause faulty operation.
- If the CONTROL terminal on the player's rear panel is connected to another component, point the remote control at that component for operation. Operation is not possible when pointed at this player.
- When using the remote control, first press the POWER switch to turn on the player's power.



## **■** SPECIFICATIONS

## General

SystemDVD system, LaserVision DIsc system and
Compact Disc digital audio system
Laser Semiconductor laser: wavelength 635 nm
Power requirements:
Power consumption52 W
Weight 10.0 kg
Dimensions
(Not including protruding cables, etc.)
Operating temperature+5°C to +35°C
(+36°F to +96°F)
Operating humidity
Operating numbers
Video Output (2 pairs)
Output level 1 Vp-p (75Ω when loaded, synchronous negative)
· · · · · · · · · · · · · · · · · · ·
JacksRCA jacks
S-Video Output level (2 pairs)
Y (luminance) - Output level 1 Vp-p (75 Ω)
fundamentes - Output level

# Digital audio characteristics

Frequency response 4 Hz to 22 kHz (DVD fs: 48 kHz) 4 Hz to 22 kHz (LD, CD) S/N ratio 115 dB (EIAJ) Dynamic range 97 dB (EIAJ) 0.003 % Total harmonic distortion Wow and flutter Limit of measurement (±0.001 % W. PEAK) or lower (EIAJ)

	•	-	•	-			
Output level	1	Vp-p	$(75\Omega$	when I	oaded,	synchronous neg	ative)
Jacks						RCA	jacks

Y (luminance) - Output level	1 Vp-ρ (75 Ω)
C (color) - Output level	286 mVp-p (75 Ω)
Jacks	S-VIDEO jacks

# Audio Output (2 pairs)

Output level	
During digital audio output	200 mVrms (1 kHz, -20 dB)
Number of channels	
Jacks	

#### Other Terminals

Optical digital output (AC-3/PCM)	Optical digital jack
Coaxial digital output [AC-3/PCM]	RCA jack
Coaxial digital output (PCM)	RCA jack
AC-3RF output (for LD)	Pin jack
CONTROL IN	
CONTROL OUT	Minijack (3.5ø)

## **Accessories**

Remote control unit	1
AAA/R03 dry cell batteries	
Audio cord	
Video cord	
S-video cable (DVL-90 Only)	i
Power cord	i
Operating Instructions	
Warranty card	

#### NOTE:

The specifications and design of this product are subject to change without notice, due to improvement.

